MODEL 1008
Manual No. TM1008A

PROPHET-T8 SYNTHESIZER

TECHNICAL MANUAL

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About This Manual and Servicing the Prophet-T8

Sequential Circuits issues this technical manual for use by qualified technicians in servicing its products. Owners should generally not attempt to service their own instruments. (It can be a very expensive way to learn electronics.) At the same time we like to give owners access to this information. This is done on condition they realize that any unauthorized service (including scaling) or modifications void the warranty.

Throughout this manual it is assumed that the reader is both familiar with operation of the instrument (see Operation Manual, SCI# CM1008), and with the functions of common linear, TTL, and CMOS integrated circuits. Anyone contemplating repair or modification work on the Prophet-T8 must already understand hybrid (digitally controlled analog) synthesizers such as the Prophet-5. For additional background on the Prophet series of synthesizers, see the Prophet System Technical Manual (TL1016B).

If you are familiar with SCI Technical Publications, you'll find this manual organized quite a bit differently from its predecessors. In the past, information has been organized topically, as procedures, theory of operation, documents, parts lists, and so on, with information concerning the various sub-systems spread throughout. This manual turns everything around; hopefully, for the better. Here, all information is organized around the actual PC-board sub-systems with which the technician must deal. The manual has the following sections:

O **OVERVIEW**
Explains the design at the block-diagram level, describes functional and diagnostic test setups, and chassis hardware.

K **KEYBOARD**
Covers all specifications and procedures regarding the keyboard mechanism.

1/2 **CONTROL PANEL & WHEELS**

3 **COMPUTER**

4/5 **DAC/SYNTH**

6 **AUDIO OUT/BACK PANEL**

7-9 **OPTICS**

10-14 **PRESSURE SENSORS**

15 **POWER SUPPLY**

And each of these sections has the following basic structure:

Documents
Schematics
Component Designator Maps
Mechanical Drawings

Procedures
- Functional Tests
- Electrical Adjustments
- Diagnostic Routines
- Mechanical Adjustments or Disassembly

Hardware Description
- Chassis-level Components
- Integrated Circuits
- Other Designated Components
- Non-designated Components

For example, all information concerning the optical system is in one section. Each section begins with the relevant schematics and parts layout diagrams, because these are needed most often. These are followed by functional and diagnostic test procedures covering that sub-system, and any mechanical or other service procedures. For troubleshooting, the theory of operation is self-indexed according to the integrated circuit designator. If you want to find out what a specific IC does, you only need to look it up by its designator, rather than dig through several pages of circuit descriptions. We have made these changes because in the real service world, where technicians must deal with perhaps hundreds of different instruments, few have the time to read cover-to-cover all of the new technical manuals which cross their bench. This reorganization should make the manual more useful as a reference tool.

Designator numbers are the labels used in the schematics and indicate the board on which they are located as well as the approximate position on the board. For example, if you wish to look at R5137 in the Oscillator B "sync" circuit, the "5" indicates PCB5. Looking at the designator map of PCB5, the resistor designator numbers increase as you scan the board from left to right, top to bottom. (Any exceptions generally indicate later modifications.)

The following table explains the designators as they appear in the following sections.

DESIGNATOR	DESCRIPTION
C	Capacitor
D	Diode
DS	Display
J	Socket
P	Plug
Q	Transistor
R	Resistor
RA	Resistor Array
S	Switch
TB	Connector cable (may be a subassembly)
TP	Test Point (not a part)
U	Integrated Circuit
Y	Crystal

Although the schematics for each PCB of the instrument are located in the various sections, they are tied together by a common labeling scheme--they are sequentially lettered "A" through "S". For example, schematic sheets "D", "E", and "F" are located in Section 3, as they all apply to Board 3. The identifying letter is found in a flag in the upper right hand corner of the schematic. Additionally, all connections which cross from one schematic sheet to another are terminated in a flag identified by the letter of the other sheet.

ABSTRACT SCHEMATIC #1
Main, Final Computers, DAC

ABSTRACT SCHEMATIC #2
VOICE and AUDIO OUTPUT

INTERCONNECT DIAGRAM
11x17
50%

O.1 OVERVIEW

This section provides a general introduction to the design of the Prophet-T8, a more detailed discussion introducing the function of each sub-system, and information about the physical organization of the chassis.

O.2 GENERAL INTRODUCTION

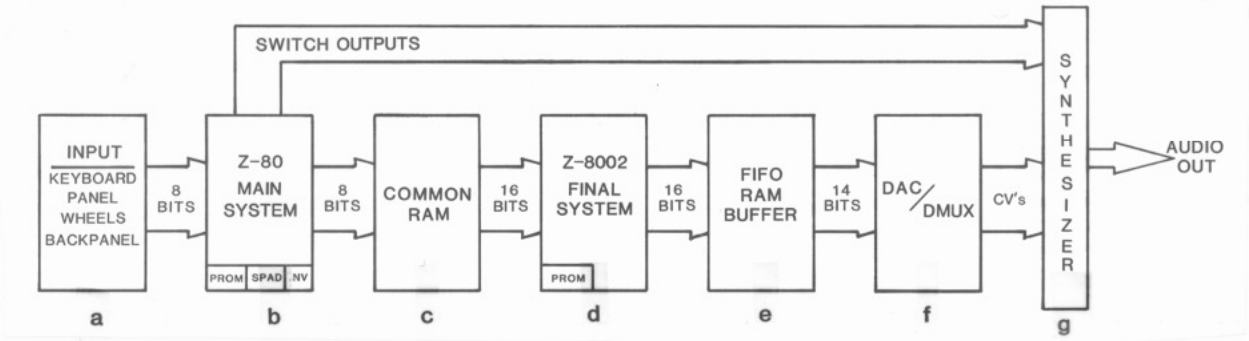


Figure O.2
GENERAL BLOCK DIAGRAM

The Prophet-T8 is a programmable polyphonic hybrid synthesizer. The term "hybrid" refers to the combination of digital microcomputer and analog synthesizer circuitry. As shown in this figure, the a) input circuitry drives the b) Z-80B eight-bit Main processor which develops keyboard and control information which it places in c) Common RAM (as well as signals which control the analog switches in the synthesizer). The d) Z-8002 sixteen-bit Final processor turns the Common RAM information into digital control words which it sends to the e) FIFO RAM Buffer. The f) DAC and Demultiplexer circuits convert these words into analog control voltages (CVs) which control the g) analog synthesizer.

Digitally processing all synthesizer control signals allows each set of control data which comprise an instrument or sound effect to be stored in Main memory as "programs," and be instantly available as a control state. Sets of real-time keyboard data are also stored in memory as "sequences." So the microcomputer primarily functions as a controller (rather than as a synthesizer).

But while the Prophet-T8 embodies this basic design philosophy of the Prophets -5 and -10, its computer system differs from these predecessors by participating more directly in the synthesis itself. Like the Prophet-600, there are no separate, integrated analog envelope generators. Instead, the Final processor calculates the exponential envelope values, integrates these with velocity and pressure information, and supplies the results as dynamic (in other words, rapidly-changing) CVs for each voice filter frequency and amplifier gain. For POLY-MOD, since the filter envelope is already "in" the computer, it is also integrated through software into the CVs for selected POLY-MOD destinations. A noteworthy side-effect of these techniques is that the familiar TRIGGER and GATE signals for each note no longer appear in the synth. (Instead you can see the envelope itself at one of the outputs of the demultiplexer.)

Several other control functions are also "synthesized" by the computer system, for example, the Left and Right modulation LFOs. When modulation destinations are enabled, the LFO is digitally summed into, for example, the oscillator frequency or pulse width (PW) CVs, or filter frequency CVs. The PITCH and MOD wheels and Glide functions are also fully digitized. The great benefit of these changes is that there is no need for Common Analog circuitry (such as in the -5 and -10) with a dozen op amp summers and precision-matched resistors.

In the conversion of these formerly analog functions into digital form, one witnesses specific examples of the predicted influence of the decreasing cost of digital memory, compared to analog hardware. But the -T8 also benefits from the higher level of integration of quality synthesizer functions offered by new analog VCA (CEM 3360) and filter (CEM 3372) ICs. The -T8 voices are identical to those in the Prophet-600, having far fewer analog components and adjustments than earlier Prophets. This all means lower price, lower power consumption, less heat, better reliability, better oscillator and filter stability, and easier service.

0.2.1 POWER-OFF NON-VOLATILE RAM PROTECTION

Please refer to page O.1, the Microcomputer Abstract Schematic. Assume that power is switched off. To maintain the integrity of the sound programs and the sequences stored in RAM, a constant voltage to the RAMs is required, and the CPU must be disabled during power-on/off transitions. BT301, a long-life lithium battery, provides Vnv (non-volatile) to U312, U316, U311, U313, and U317 which are the five 6116LP-3 2K x 8-bit static RAMs. (Actually, only four of these are for non-volatile data. The fifth is for Scratchpad Memory.)

Vnv also powers U302, containing the Schmitt triggers which operate the power detector, and RAM Write Protect gates U306 and U307 which prevent altering RAM contents while power is switched on or off.

O.2.2 POWER DETECT AND RESET

When power is switched on, Vpd from the power supply will after a brief delay cause the two complementary RESET signals to toggle to their false states. This initializes both CPUs, the MIDI UART, Arbitration Logic, FIFO buffer, a Miscellaneous Output Port (U319--drawn next to the LED Matrix), and enables RAM access through the U306/7 Write Protect gates.

When the low-voltage supply has charged, Vunreg appears. It takes over the duty of powering all NV circuits--so they can operate at full speed.

When power is switched off, Vpd will fall instantly, toggling both reset lines back to their true state. Of greatest importance, the RAM Chip Selects are disabled to prevent random memory access instructions from being performed during power-down (which could alter RAM contents).

O.2.3 SYSTEM CLOCK

U323 6 MHz Clock motivates the two CPUs and synchronizes the high-speed Arbitration Logic. The Dividers generate four slower clocks: for the Tune Time Counter, A-440 divider, UART (which internally divides that down to the 31.25 kBaud MIDI rate), FIFO Timing Logic, and Interrupt system.

O.2.4 MAIN SYSTEM

The Z-80 Main processor handles the keyboard, control panel inputs, MIDI, and program and sequence data to constantly update Common RAM with current data required by the Z-8002 Final processor. The Main processor system (the term "system" emphasizes the combination of hardware and software) consists of the Z-80 Main CPU, U322 2764 8 kByte EPROM, the five NV RAMs mentioned above, and the MIDI UART. The Main CPU executes the program permanently residing in the Main EPROM. This determines how and when the various input devices--keyboard, switches, knobs, and MIDI--are "scanned," how data resulting from these scans are processed, and how the output devices--LEDs, synth switch latches, MIDI and Common RAM--are "strobed" with the processed data.

The computer is organized primarily around its Data Buss, over which all information passes, one byte at a time. The activity of the various devices connected to the Data Buss is coordinated by Chip Select (CS) signals which the computer generates through its Memory and Input/Output (I/O) Port decoders. The appearance of the CS signal causes the "buss drivers" to place data on the Data Buss, or causes the "latches" to take data off of the Data Buss.

Main Address Buss lines AM0 through AM12 define locations in several of the memory-mapped devices. U305 Memory Decoder selects ROM or RAM according to the most-significant bits of the address buss. To access memory, -MREQ--which indicates that the buss holds a valid memory address--must be low (true) and -RFSH--which indicates that the buss holds a valid refresh address--must be high (false).

All EPROM operations are memory-read. Whether RAM operations are read or write is indicated by the -RD or -WR signals. (UART transmit/receive operations are determined by the AM2 line.) Velocity and pressure information is always written to Common RAM, but control knob and switch information is only sent in Edit and Manual modes. In Preset mode, programmed parameters from non-volatile Main memory take their place. The current status of the controls--on/off for switches, position for knobs--is always maintained in the "Edit" table in Scratchpad RAM. In Preset mode, the selected program is written into the "Current" table in Common RAM which controls the synthesizer. If one alters a knob or switch setting in the Edit table, that change is written to the "Current" table, and will show up as a different sound. The original program remains unaffected, unless you specifically record the Current table back to the program location in NV RAM.

Input/output port selection follows similar principles as memory interface, only the address lines define ports which are validated by -IORQ (instead of -MREQ). -IORQ (Z-80 pin 20) connects to U303/04 I/O decoders. With regard to I/O, -RD true defines an input operation, typically from data buss drivers which hold data from the keyboard, or control panel. -WR defines an output to a latch or register.

O.2.4.1 MAIN INTERRUPT

The 1-kHz (actually 0.98-kHz) interrupt clock is provided to both processors. The most critical processing activity, keyboard scanning, must be done at this rate to give sufficient resolution for velocity. The Z-80 has two interrupt inputs: -INT (Maskable Interrupt) and -NMI (Non-Maskable Interrupt). The first is constantly clocked, the second is used only for MIDI (see below).

Each low pulse from the Interrupt Flip-Flop (INT FF) forces the Main processor into its Interrupt routine. (Actually because this interrupt input is "maskable," there are some rare times when the CPU will ignore it.) First -M1 (a CPU cycle indicator) goes low, with -IORQ true causing a low -INT ACK which resets the FF. The INT FF has to be reset when first entering the interrupt state so the processor doesn't keep getting interrupted. The Main CPU then scans the entire keyboard. It will scan the pressure sensors of keys which are down. (There is no reason to waste time scanning all the pressure sensors.) To prevent flickering, the front-panel LEDs are also strobed at this constant rate. The time between the end of interrupt processing and the appearance of the next interrupt leaves a "background" period for accomplishing less real-time dependent tasks such as reading control knobs and switches. These scans therefore occur over several interrupt cycles.

O.2.4.2 MISCELLANEOUS INPUT

Most Main system inputs are shown at the left of the abstract schematic. Working up from the bottom of the page, -CSIO4 selects U320 Miscellaneous Input Port which brings in squared-up pulses from the Cassette Comparator, and active-low signals from the three footswitches and the back-panel RECORD switch.

O.2.4.3 SWITCH MATRIX INPUT

The matrix switch scanning method is widely used. The control switches are wired in a matrix whose columns are enabled by bits latched from the Matrix Decoder (which is selected by CSO12H. Data generated by rows of closed switches are read by the Switch Input Driver.

Pressing a switch routes the high signal for the column to a selected row. The diodes wired throughout allow "n-switch rollover"--which is the pressing of any combination of switches--by isolating each switch. If the diodes were not present, signals from closed switches would pull other columns high.

O.2.4.4 MULTIPLEXER INPUT

Under the keybed are pressure sensors for each key which are actuated after the key reaches the bottom of its travel. The pressure sensors are miniature variable resistors whose resistance decreases with increased pressure. The control knobs are potentiometers which provide a wiper voltage analogous to their position.

As required for scanning the switch matrix, a combination of output and input processes are actually required for the computer to read the pressure sensors and knobs. The multiplexer allows the Main processor to select and read each specific analog voltage. Each of the 4067 ICs has sixteen inputs, and each of the 4051s has eight inputs. All of their outputs are summed by U107. U102 Address Latch provides a binary number (0-15 decimal) to all the multiplexer ICs, to select one of its inputs. But only one multiplexer IC is enabled at a time, by low signals from U103 Strobe Decoder. The continuous combination of these two codes select a pressure sensor or knob to be connected to the Vmux line which goes to the eight-bit Analog to Digital Converter (ADC). (The last Prophet which included an integrated ADC was "Rev 2" of the Prophet-5.) For accuracy, the ADC has its own voltage reference, Vref, formed by buffering a voltage divider. To actually read the knob, the computer issues the Chip Select which causes U106 to drive the ADC value on to the Data Buss.

Notice that during normal operation, if no keys are held, the pressure mux is not scanned. During each interrupt the Main processor reads the pressure sensors of keys that are down, and checks either the PITCH or MOD wheel and one other knob for motion. Because the interrupt loop is 1 ms, each wheel is sampled every 2 ms. This rate is fast enough to detect typical real-time performance. If a difference is detected in the PITCH wheel, oscillator pitches are raised or lowered accordingly. A difference in the MOD wheel increases or decreases modulation amounts.

When a program is selected, equivalent pot values (and switch settings) are transferred from the program area of NV RAM to a "Scratchpad" area, from which the values are output to the Common RAM as principal variables for the equations which result in the appropriate CVs for the synthesizer. Also in Scratchpad the CPU maintains another table of the pot values corresponding to wherever the knobs currently happen to be set.

Since there are 35 knobs, each of the other pots is scanned every 35 ms, (if no pressure is applied and no knobs are moving). If one of these knobs is moved, the CPU learns this by comparing the ADC result with the Current table. When the knob has "found" the current program value, this activates Edit mode, which means further pot motion will also update the main Scratchpad table, thus change the sound.

During multiplexer address changes, the computer inhibits all multiplexer ICs. This prevents switching spikes from entering the ADC.

O.2.4.5 KEYBOARD INPUT

The -T8 uses optical sensors to eliminate the switch bounce which would normally interefere with the process of accurately reading wide ranges of velocity with mechanical switches. The Main processor scans the keyboard each interrupt cycle. The 19 strobe signals needed to scan the keyboard are produced by decoding the lower four bits of the data buss with the Strobe Decoder, and latching the upper four bits with the Strobe Latch. After inversion by the driver, these strobes pull-down the cathodes of the upper and lower infra-red LED emitters, turning them on. When the key is at rest, the vane connected to the hammer blocks the optical path between the upper and lower emitters and their accompanying phototransistor detectors. Both sensors send a high signal to the computer. Pressing the key causes the hammer vane to move downward, so that when the vane has moved 30% of its range of travel, it opens the

upper optical path. The computer sees this low signal as a Note On event, then watches for how many interrupt cycles it takes for the lower optical path to open--signifying that the vane has reached 70% of travel. The shorter the time, of course, the greater the velocity. Release velocity is also measured.

O.2.4.6 LED MATRIX OUTPUT

It takes two output operations to light one LED in the LED Matrix. One is data from the Source Latch which is buffered by a transistor array. The other output is from the Matrix Decoder (shared with the Switch Matrix), which is inverted by the 2003s to sink the LED current. Only the LEDs which are in the coded Source-Sink path will light. As mentioned, the LEDs are scanned at the constant interrupt rate to prevent flickering.

O.2.4.7 MISCELLANEOUS OUTPUT

Bits from latch U319 go out the back panel as cassette data, turn on the A-440 circuit, and enable the RAM Write Protect logic.

O.2.4.8 SYNTH SWITCH/PROGRAMMED VOLUME OUTPUT

The synthesizer voices contain numerous solid-state analog switches which close when their control lines are driven high by data latched from one of these four latches (U359/60, U365/66). In Preset mode these switch signals are set by the current program. In Edit or Manual Modes these signals directly follow their corresponding switch or knob (if turned "live") on the control panel.

U325 Programmed Volume Latch sends four control bits each to the Left and Right Audio Output stages. These control volume through the Digitally-Controlled Attenuators (DCAs).

O.2.4.9 MIDI I/O

The MIDI UART allows the -T8 to communicate keyboard and program control information (as selected from the front panel) via serial data input and output. As the keyboard is played this data is converted to the MIDI protocol and sent to the UART one byte at a time for transmission to any receiver which may be connected. When the UART receives MIDI data, it signals UART RDY to the Main CPU Non-Maskable Interrupt (NMI). This forces the CPU to suspend whatever it is doing and retrieve the data from the UART, so that the UART will be free to receive more data.

O.2.5 COMMON RAM AND ARBITRATION

Optimized toward the Final processor, Common RAM is sixteen bits wide. Common RAM holds the results of the Main Processor's input operations. This includes the ever-changing keyboard velocity and pressure inputs, the two wheels, MIDI, and the less-often-changing control and synthesizer switches. The Main processor writes control data to the Common RAM in the formats needed by the Final Processor. For example some of the knobs act as plus/minus controls. In such cases the Main takes the 00-FFH number from the ADC and converts it to a plus/minus two's complement sixteen-bit number with the correct weighting. The eight-bit Z-80 can only access one byte at a time of course, so its Common RAM logic is a little more extensive than the sixteen-bit Z-8002's because upper and lower bytes have to be selected.

The Main and Final Data busses interface Common RAM through bidirectional Main/Common or Common/Final transceivers. The Address Buss Selector determines which Address Buss (Main or Final) selects the Common RAM Address. The direction of data to or from the processors, and the addressing of data by the processors is governed ultimately by the Arbitration logic. It prevents the Main and Final processors from conflicting in their use of Common RAM.

For the Arbitration logic, both processors have request (REQ) signals which are decoded memory addresses, enable (EN) signals which turn on their Common RAM transceivers via the Main/Final logic select circuits, and WAIT signals which tell them to pause. The Final processor is given priority. For example if the Final wants to read Common RAM, it sends a request to the Arbitration logic. The logic prevents the Main from writing by issuing the Z-80 WAIT signal. (In reality, the Main and Final programs are synchronized so tightly that neither processor enters a wait state during normal operation.)

O.2.6 FINAL PROCESSOR

The Final processor refers to Common RAM for keyboard and control data from which it calculates the oscillator pitches, digital envelopes, LFOs, and Glide into six final CVs for each of the eight voices (48 total plus a few miscellaneous CVs).

The Final processor system consists of the Z-8002A, two 2732 EPROMS (4K words), the 8253-5 Counter/Timer for Tune and A-440, and the 64-word deep First-In-First-Out (FIFO) which is decoded as a single memory location. The Tune control latch is also memory-mapped. The Final Address buss is latched off of the Final Address/Data Buss by a latch driven by the -AS (Address Strobe) signal.

The Final processor reads a word from U350 and U351 EPROMs by decoding a Chip Select through the Memory Decoder when -MREQ is true. Program instructions are placed on the buss when -DS is true. The second output from the Memory Decoder is gated with -DS to create the FIFO -CS. Similarly, a third line selects U345 Tune Control latch. This latch is memory-mapped because tuning requires greater speed than would be achieved by I/O mapping.

The Status Decoder generates the single I/O select which allows writing to and reading from the Timer/Counter. It also clears the Non-Vectored Interrupt (NVI) Flip-Flop. The Final processor is interrupt-driven because it must perform the real-time task of

velocity and envelope calculation. It counts interrupts and clears them with the -NVI (Non-Vectored Interrupt) ACK signal from the Status Decoder. The CPU responds only to every third clock, with the same routine for CV output and calculation. This gives the envelopes a basic resolution of 3 milliseconds. (This is the minimum time increment for each envelope period--attack, decay, or release.)

In background mode, the Final CPU processes key on/off information which has been received from the Main system.

O.2.6.1 DAC, DEMULTIPLEXER, AND SAMPLE/HOLDS

All CVs which control the synthesizer pass through the Demultiplexer. The Demultiplexer can be thought of as a spinning rotary switch which momentarily routes a specific analog voltage from the fourteen-bit digital-to-analog converter (DAC) to each sample/hold (S/H). These devices sample the DAC voltage and hold it until the next sample appears.

At the beginning of each interrupt cycle, the Final CPU does a high-speed block move of 59 sixteen-bit words to the FIFO. Output Ready (OR) goes high. The processor continues with other tasks while the Timing and Sync Logic synchronizes reading the FIFO output to the DAC and Demultiplexer.

The fourteen bits from the FIFO cross over from PCB 3, and are buffered into the active-low inputs which the DAC requires. The DAC has a basic range from 0 to 10V. No trimmer is required. U445 converts the output current to voltage, Vdac, which is distributed by the Demultiplexers on PCBs 4 and 5.

During each interrupt reading of 59 values from the FIFO, Vdac assumes the value of each S/H. The Demultiplexer is synchronized so that the correct S/H is strobed at the precise time that Vdac assumes the corresponding value. The Timing and Sync logic selects the appropriate S/H by providing an address from the Sample/Hold Decoder, which selects only one Demultiplexer channel at a time.

Note that these voltages are dynamic (constantly changing) to the degree the envelopes, velocity, and pressure and LFO-modulation are engaged. To easily obtain a clearer understanding of DAC function, it will be useful to actually observe Vdac on an oscilloscope, while exercising various keyboard and control operations.

There are two main types of CVs: polyphonic and monophonic. Polyphonic CVs are independent for each voice. Only with separate CV lines can the keyboard and various modulation systems have control over individual voices. In this class are the six separate OSC A, OSC B, FILT, PWA, PWB, and AMP CVs which, for the Left voices, are demultiplexed by U436-38. In contrast, U439 demultiplexes the monophonic RES, MIX NOISE, MIX A, MIX B, and POLY-MOD OSC B CVs which are common to all four Left voices. Similar to the switch bits, these monophonic voltages reflect basic program parameters.

The basic S/H circuit for each of these consists of a low-leakage capacitor and a BIFET opamp, which has an extremely high input impedance. The 4051 momentarily connects Vdac to the S/H. The capacitor charges to the value of Vdac. It retains this value while the demultiplexer strobes all the other S/Hs.

O.2.6.2 A-440

The A-440 signal is created by merely dividing 3 MHz by the appropriate integer. Both the enable signal and the A-440 product go the Audio Output circuitry on PCB 6.

O.2.6.3 TUNE

The Tune system is responsible for the entire performance for the instrument in the sense that without its corrective influence, the sixteen oscillators could not by themselves be expected to constantly stay in tune, due to temperature drift and component aging. Basically, each time the TUNE switch is pressed the system precisely-measures oscillator and filter (in resonance) frequencies over a nine-octave range, and learns the exact CVs required to produce perfectly-tuned octaves. During tuning, squared-up oscillator or filter pulses from the Tune Comparator (see below) are gated by the Tune latch through an AND gate to the Cycle Counter. This timer section is programmed to function as a one shot which at first goes low, then high after a programmed number of oscillator (or filter) cycles. This action gates MI (Micro In) in the processor, and the Total Time counter which accumulates the number of 3-MHz pulses corresponding to the programmed number of oscillator cycles. This provides very accurate period measurement of frequency. The differences between the theoretical and actual CVs which produce specific intervals are called tuning "biases." When playing, these biases are independently recalculated for each note and each oscillator, so that all sixteen oscillators and eight filters remain in tune at every note throughout their range. In other words the computer measures the oscillator or filter error at octaves, then while you play corrects the note to which that oscillator happens to be assigned.

O.2.7 SYNTHESIZER

Looking now at the Analog Abstract Schematic (page O.2), each voice contains 2 CEM3340 voltage controlled oscillators (VCO) A and B and the CEM3372 voltage-controlled combination mixer, 24 dB/octave resonant low-pass filter, and amplifier. The voices have been considerably simplified by the integration of voltage-controlled mixer, filter, and amplifier functions into this IC. (The voice signal flow is described in general in the Operation Manual and in more detail below.)

O.2.7.1 OSCILLATORS

Each oscillator has independent frequency and pulse-width Sample/Holds from the CV demultiplexer. For Poly-Mod (modulation of each OSC A by the OSC B in the same voice), two switches add the OSC B signal to the OSC A frequency and pulse-width CV inputs. Two output switches route the OSC A sawtooth and triangle waveshapes to the filter. The pulse waveshape is switched on and off by simply applying enough CV to drive it all the way to dc. OSC A SYNC to OSC B is switched on and off by a bit which toggles high or low voltage from a dual-pole switch. OSC B is similar to OSC A except that for OSC B LFO applications a switch adds a very low CV to the frequency inputs, lowering the oscillators' ranges of operation. The POLY-MOD VCA adjusts the amount of OSC B fed to the two POLY-MOD OSC A switches already mentioned, and the

POLY-MOD FILTER switch. Note that the POLY-MOD filter envelope source has no path in the voice--it is applied via the OSC A FREQ, PW, and FILTER FREQUENCY CVs.

The oscillators and filter operate in exponential (as opposed to linear) control mode, scaled at 1/2 volt per octave. This means an OSC FREQ CV change of 1/2V produces a pitch change of one octave, and is a departure from our previous practice of using 1V/octave. Doubling the sensitivity of the oscillators allows the basically 5-V DAC to still control a ten- (instead of five-) octave range. Actually OSC A and B range nine octaves, following up to 2.5V (five octaves) provided by the keyboard and up to 2V (four octaves) provided by the FREQUENCY knobs.

The VCO itself is of course a complex of other circuits. Basically, the summed CV drives an exponential control current generator, which charges an external timing capacitor. The increasing positive charge on the capacitor produces the ascending portion of the triangle wave by direct integration. When this charge reaches a specific level, a comparator switches-in a discharge path for the capacitor, producing the descending portion of the triangle wave. The sawtooth is obtained from the triangle via another comparator and switch. The pulse wave is created by a comparator which toggles as the sawtooth level matches the pulse width CV input.

Pitch accuracy amid varying temperatures is the main challenge of VCO design. As it heats and cools, the exponential control current generator charges the timing capacitor more or less quickly, altering the oscillation period (pitch). The stability of the Prophet-T8s oscillators results from the 3340 including a temperature compensation (TEMPCO) circuit which has the same temperature characteristics as the exponential generator, but which counteracts drift by making the necessary adjustment through the precision multiplier stage. (As opposed to stability, the oscillator accuracy depends on the TUNE system.)

O.2.7.2 MIXER/FILTER/VCA

Both oscillator outputs are ac-coupled to the filter. The oscillator levels have separate MIX CVs. A third input is the noise level as adjusted by the Noise VCA for that side (Left or Right). The Filter CV from the computer (Sample/Hold) is highly dynamic. It may be supplemented by the output of OSC B, if the POLY-MOD FILTER switch is on. Filter resonance is controlled for either the left or right sets of four voices. The resonance amplifier is internally compensated to provide a fuller sound than our previous filters. The AMP CV is also highly dynamic--it includes the Amplifier Envelope.

The four voices on each side of the -T8 are summed and sent to the Left and Right Final VCAs. When on, A-440 is summed-in at this point. Controlling these VCAs, the BALANCE and MASTER VOLUME knobs create the basic CVs which are attenuated by the Left and Right Digitally-Controlled Attenuators (DCAs), as programmed by data from the Programmed Volume Latch (in the Main system). This arrangement allows the computer to completely disable audio output when necessary, for example, during TUNE.

The VCA outputs are buffered to line impedance and summed for a convenient monophonic output.

O.2.7.3 TUNE SELECT

Unlike the earlier Prophets, the -T8 contains no Tune Multiplexer. Instead, for tuning, the Programmed Volume is switched off and the computer selects the oscillators and filters to be tuned.

Returning to the Voice Summers, the Tune system draws its signals from the voice by way of the Tune Side Select switch (which is controlled by the M0 output of the Final CPU) on the input to the Tune Comparator. The Comparator output is enabled by the TUNE EN bit, and drives the Cycle Counter in the Tune Circuit.

The TUNE system uses the Final system as a frequency counter. The tune system tunes each oscillator and extracts an offset (or bias) value for each octave at (eight) "A"s. To save time, two values for the lowest octaves are extrapolated--for a total of 10 octaves. Corrections for each oscillator's error are averaged while playing.

The filters are tuned at 880 Hz only.

O.3 TESTING PROCEDURES

The term "tests" applies to two different types of activities:

> A functional test involves operation of user controls to verify that the Prophet-T8 is performing within specifications. Any failures should be documented.
>
> A diagnostic test is performed after the unit is opened. It involves activating alternate programs which assist troubleshooting the various sub-systems.

Functional testing procedures relevant to each sub-system are found in each section of this manual.

The diagnostic procedures are also organized by sub-system. In software however, the diagnostic tests are divided between the Main and Final computer systems. And the Main diagnostics are divided into two banks. Here is how the tests are organized and where they can be found:

	Page
Main Diagnostic Tests (contained in PROM "DT8_4")	
Set-up Instructions	3.14
Bank 1 computer system diagnostics	
M1 I/O port test	3.16
M2 LED test	1/2.11
M3 Local RAM test	3.17
M4 Common RAM test	3.17
M5 ADC test (pots, pressure sensors, wheels)	1/2.11, 10-14.7
Bank 2 keyboard tests for calibration and debugging	
K1 Test of unmounted optical system	7-9.11
K2 Single step test of key optics	7-9.10
K3 Looped scan of pressure sensors	10-14.8
K4 Single step test of pressure sensors	10-14.9
K5 Looped scan of optical system	7-9.9
K6 Pressure sensor slope analyzer test	10-14.10
Final Diagnostic Tests (contained in resident FINAL EPROMS)	
Set-Up Instructions	3.18
F1 MO TOGGLE	3.19
F2 COMMON RAM	3.20
F3 DAC	4/5.34
F4-17 BIT TESTS	4/5.35

O.3.1 PREPARATION FOR FUNCTIONAL TESTS

CAUTION! Do not connect Prophet-T8 to power and do not switch power on until directed!

CAUTION! Do not switch line voltage while instrument is on or connected to the line.

1. Check that the line voltage selector on the back panel is set to match the local line voltage.

   Do not attempt to test the voltage select switch without having (both) proper line voltages available.

   Although the switch is marked 110V/220V, the transformer and power supply are rated 115V/230V.

2. Check that the fuse is correct for the selected line voltage:

   110V (115V): 3/4A slo-blo
   220V (230V): 1/2A slo-blo

3. Switch off power to audio monitor system and connect LEFT and RIGHT to it.

4. Connect the detachable power cable between the -T8 and power source.

5. Switch -T8 power on, then switch monitor system power on (if used).

   If the power supply primary is OK, the power switch lights. On the front panel, only TUNE is lit. It stays lit for 25 seconds, then the control panel lights normally. LINK, PRESET MODE, and RIGHT PROGRAMMER are on. The PROGRAM display shows RIGHT PROGRAM 11 and whatever LEFT PROGRAM number is linked to the RIGHT.

   If no LEDs light, check or replace fuse and try again. (Of course there is a slight chance that the TUNE LED itself is bad.)

   If the TUNE LED does not go off, or the front panel fails to light normally, there is a computer problem which may prevent further testing. (See the computer diagnostic procedures.)

6. To obtain a pilot tone, switch A-440 on, and adjust MASTER VOLUME and the loudness of the monitor system (if used).

   For optimum signal-to-noise ratio, keep MASTER VOLUME raised, while reducing the monitor system gain.

7. If the control panel has normal indications but the A-440 tone can not be heard (directly from AUDIO OUT with headphones) peform the AUDIO OUT test on page 6.3, then look into the final VCA and audio output circuitry.

O.3.2 CASSETTE INTERFACE FUNCTIONAL TEST

Urge customers to save their current programs and sequences on cassette before leaving instruments for service. If the owner has successfully backed-up current programs and sequences, it is obviously not necessary to test the interface.

On the other hand, the cassette interface may be the only service complaint. 80% of cassette interface problems are due to incorrect record or playback levels. As required, instruct the owner in correct use of the interface. (This support is actually the dealer's responsibility.)

Note: If it is not known whether the owner has backed-up, or whether the interface works, test it as follows, before recording anything in the memory. (If you do this the owner may be forever grateful.)

To save programs and sequences:

1. Connect CASSETTE TO TAPE to the recorder input.

2. Connect CASSETTE FROM TAPE to the recorder output.

O.3.2.1 SAVING 128 USER PROGRAMS

1. Check back-panel RECORD switch is set to ENABLE.

2. Insert cassette into recorder and rewind to start of tape.

3. Zero the tape counter.

4. If the recorder is equipped with noise reduction, switch noise reduction off.

5. Check that the LEFT and RIGHT PROGRAM displays show two digits.

6. Switch RECORD MODE on.

7. Place recorder into record.

8. Wait five seconds.

9. Press SAVE TO TAPE.

10. Use the pilot tone which appears to adjust record level to 0 dB (or slightly into the red). Do not adjust level while the -T8 is sending data to the recorder. (It may be necessary to do a trial loading, or two, to get the correct recording level.)

11. When LOAD FROM TAPE blinks, stop recorder.

O.3.2.2 VERIFY USER PROGRAMS

1. LOAD FROM TAPE is blinking. Rewind tape to index number.

2. Check playback level.

Rule-of-thumb for playback level is 75% of full volume for portable recorders.

3. Place recorder into play and wait until the pilot tone appears.

4. Press LOAD FROM TAPE.

5. When LOAD FROM TAPE goes out, stop the recorder. The program recording has been verified. The -T8 control panel will return to normal.

6. If LOAD FROM TAPE LED instead blinks, a tape error has occurred. Try adjusting playback volume and verifying again.

O.3.2.3 SAVING EIGHT USER SEQUENCES

1. Make a note of the tape index following the program file (or use a new cassette).

2. Switch on SEQUENCER SELECT/STOP.

3. Switch RECORD MODE on.

4. Place recorder into record.

5. Wait five seconds.

6. Press SAVE TO TAPE.

7. Use the pilot tone which appears to adjust record level to 0 dB (or slightly into the red).

8. When LOAD FROM TAPE blinks, stop recorder.

O.3.2.4 VERIFY USER SEQUENCES

1. LOAD FROM TAPE is blinking. Rewind tape to index number.

2. Check playback level.

Rule-of-thumb for playback level is 75% of full volume for portable recorders.

3. Place recorder into play and wait until the pilot tone appears.

4. Press LOAD FROM TAPE.

5. When LOAD FROM TAPE goes out, stop the recorder. The sequence recording has been verified as correct. The -T8 control panel will return to normal.

6. If LOAD FROM TAPE LED instead blinks, a tape error has occurred. Try verification again.

0.3.2.5 LOAD FACTORY PROGRAMS (OPTIONAL)

1. If you are experienced enough on Prophets to work with the user's programs, fine. Otherwise load the standard Factory Programs.

> Note: While the functional test procedures in this section can be performed without using any specific factory programs, it is usually not necessary to reprogram the -T8. However, service complaints may concern specific programs. Therefore to filter out all the potential variables in a user program, it may be more convenient for you to use the Factory Programs with which you may already be familiar.

2. Insert Factory Program cassette (SCI #858) into recorder and rewind to beginning.

3. Check playback level.

> Rule-of-thumb for playback level is 75% of full volume for portable recorders.

4. Switch RECORD MODE on.

5. Place recorder into play and wait until the pilot tone appears.

6. Press LOAD FROM TAPE.

7. When LOAD FROM TAPE goes out, stop the recorder. The Factory Programs have been loaded. The -T8 control panel returns to normal.

8. If LOAD FROM TAPE LED instead blinks, a tape error has occurred. Try adjusting playback volume and loading again.

9. If desired, load factory sequences.

0.3.2.6 AFTER TESTING, RELOAD USER PROGRAMS AND SEQUENCES

1. To reload programs, follow Factory Program loading instructions, above.

2. To reload sequences, repeat, except switch on SEQUENCER SELECT/STOP before RECORD MODE.

3. If desired, switch back-panel RECORD switch to PROTECT.

O.4 MECHANICAL PROCEDURES

WARNING! You are responsible for the safe operation of this instrument under service conditions. Incorrect grounding practices can create lethal shocks. Scaling and other service operations must be performed with power on. Under these circumstances lethal voltage is present in the power supply primary area. Switch power off before disconnecting or connecting any circuitry, or removing or installing printed circuit boards (PCBs), integrated circuits (ICs), or other parts.

NOTE: Whenever the cover is removed, light may leak into the Optical system and cause erratic operation. Always verify computer problems with the cover on.

NOTE: The diagnostics contain destructive memory tests. Before proceeding, be sure that the owner's custom programs are backed up on cassette. (If necessary, refer to pages O.17-19.)

O.4.1 REMOVING THE TOP PANEL

CAUTION! Switch power off before any disassembly.

This procedure provides access to the Computer (PCB 3) and Voice Boards (PCBs 4 and 5), for scaling or diagnostics.

1. Remove five screws along front edge of top panel.

2. Remove five screws along rear edge.

3. Grasp rear edge of top panel and tilt it up towards you.

4. Lift top panel off and set it aside (where it won't get scratched!).

NOTE: For PCB identification see the Interconnect Diagram, page O.3

O.4.2 RAISING THE COMPUTER AND VOICE BOARDS

PCBs 3, 4, and 5 are hinged along their rear edges, and can be operated as a unit while tilted up for troubleshooting or to allow access to the power supply, audio output, and parts of the keyboard.

1. Remove the top panel (see page O.20).

2. To raise the boards, remove the four screws along the front edge of PCB 3, and the three screws along each front edge of PCB 4 and PCB 5. (Early -T8s have quarter-turn fastners on the PCBs.)

The boards are all interconnected, so they all have to be raised at once.

3. Work carefully. You don't want to drop screws into the keyboard action.

4. Raise all three boards at once and prop them up. They rest safely when tilted towards the back at about a fifteen-degree angle.

CAUTION! The keyboard optical system is quite sensitive. Do not touch or otherwise disturb the sensors. If you are not an experienced technician, look but don't touch!

Note: When operating with the top boards raised, ambient light may cause the keyboard to behave erratically. For example, when the TUNE routine ends, often some random notes will be played briefly. If the light is very bright, information overload may stall the computer entirely--causing the control panel and keyboard to stop working. For normal operation with boards raised, it will be necessary to fashion a suitable shield out of cardboard, as shown below. For final keyboard testing, the top boards must be lowered, and the top panel placed back on (but not necessarily secured).

Figure O.4.2
RAISED TOP BOARDS

5. When lowering the boards, check that cabling lays behing the optics boards, that it does not interefere with the optics, or the travel of the key vanes.

O.5 CHASSIS HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
O.5.1		Original Package	
		CL1008	OPERATION MANUAL
		E-086	POWER CORD
		S-064	DUAL FOOTSWITCH
	Preprogrammed Tape	858	-T8 FACTORY PROGRAMS
		Q-034	SHIPPING CONTAINER
O.5.2		Chassis	
J6	Wheel Cable Conn.	J-056	5-PIN HOUSING
		P-031	POLARIZING PIN
		P-049	SOCKET PINS
W1	Control Panel Power	Z-281	PCB 1 to 15 WRG SUBASSY
"	Each end of W1	J-040	6-PIN JACK
"	For J-040	P-028	GOLD SOCKET CONTACT
W2	Control Panel Cable	E-142	17" 16-PIN RIBBON
W3	Volume/Balance Control	Z-286	PCB 2 to 6 WRG SUBASSY
"	Each end of W3	J-069	6-PIN HOUSING
"	For J-069	P-049	SOCKET PINS
"	Use at both pin 1s	P-031	POLARIZING PINS
W4	Keyboard Cable	E-141	13" 16-PIN RIBBON
	The cable (W4) between PCB 3 and PCB 9 carries the Main Data Buss, +5Vd, two Output Chip Selects (CSO), and one Input Chip Select.		
W5	Audio Control Cable	E-144	27" 20-PIN RIBBON
W6	Voice Control Cable	E-145	12" 40-PIN RIBBON
O.5.3		Cosmetic/Performance	
	PROGRAM Windows (2)	M-002	1.5" x 2" RED PLEXIGLASS
	Progammable Knobs	M-396	LOW-PRO KNOB BLK
	Non-Prog. Knobs	M-400	LOW-PRO KNOB SILVER
	Wheel	M-352	MOLDED WHEEL
	PITCH wheel detent	M-073	TENSION CLIP
		PL008-2A	-T8 LABEL
		PL008-3A	SCI LABEL
	Panel Bottom Edge (3.5')	M-159	3/16" WIDE FOAM TAPE
		M-320	LARGE RUBBER FEET
O.5.4		Wood	
		WD008-1B	UPPER CHANNEL WOOD
		WD008-2B	FRONT RAIL WOOD
		WD008-3A	LEFT WOOD SIDE
		WD008-4A	RIGHT WOOD SIDE

HARDWARE DESCRIPTION

FUNCTION	SCI PART #	PART DESCRIPTION
O.5.5	Metal Work	
	M-204	PITCH WHEEL BRACKET
	MW000-1A	MOD WHEEL BRACKET
	MW008-1A	TOP PANEL
	MW008-2B	CONTROL PANEL
	MW008-3C	BOTTOM PANEL
	MW008-4A	HINGES
	MW008-5A	FRNT PNL UPR BRKT
	MW008-6B	WHEEL BOX
	MW008-7B	RIGHT PANEL BOX
	MW008-8A	FRONT RAIL BRACKET
	MW008-9C	HEATSINK
	MW008-10B	UPPER CHANNEL
(Only used for MW008-9B.)	MW008-11A	HEATSINK SPACER
O.5.6	Wood/Sheet Metal Screws	
	M-025	#6 x 5/16 BLK FH PHIL
	M-209	#6 x 3/8" BLACK PAN PHIL
	M-368	#6 x 5/8 BLK PH PHIL
Side Cable Clamps (4)	M-430	#6 x 3/4 HEX SHT MTL
Keyboard-to-Chassis	M-441	#8 x 5/8" BLK HEX SHT MTL
	M-445	#8 x 3/4" HEX SHT MTL
O.5.7	Machine Screws	
	M-199	4-40 x 1/4" BLK PH PHIL
	M-100	4-40 x 3/8" FLAT HD PHIL
	M-428	4-40 x 1/2" PH PHIL
	M-071	6-32 x 1/4" PAN HD PHIL
Control panel to wheel box	M-473	6-32 x 1/4" BLK FLT HD PHIL
	M-156	6-32 X 3/8" CNTRSNK PHIL
	M-175	6-32 x 3/8" BLK PH PHIL
	M-050	6-32 x 1/2" FLT HD PHIL
	M-390	6-32 x 1/2" BLK FH PHIL
For wheels	M-070	6-32 x 1/2" SET SCREW
	M-397	6-32 x 7/8" PAN HD PHIL
	M-403	8-32 x 3/8" BLK PH PHIL
Top Panel (10)	M-418	8-32 x 3/8" BLK FH PHIL UND
	M-161	8-32 x 3/4" BLK PH PHIL
	M-419	8-32 x 1" BLK FH PHIL

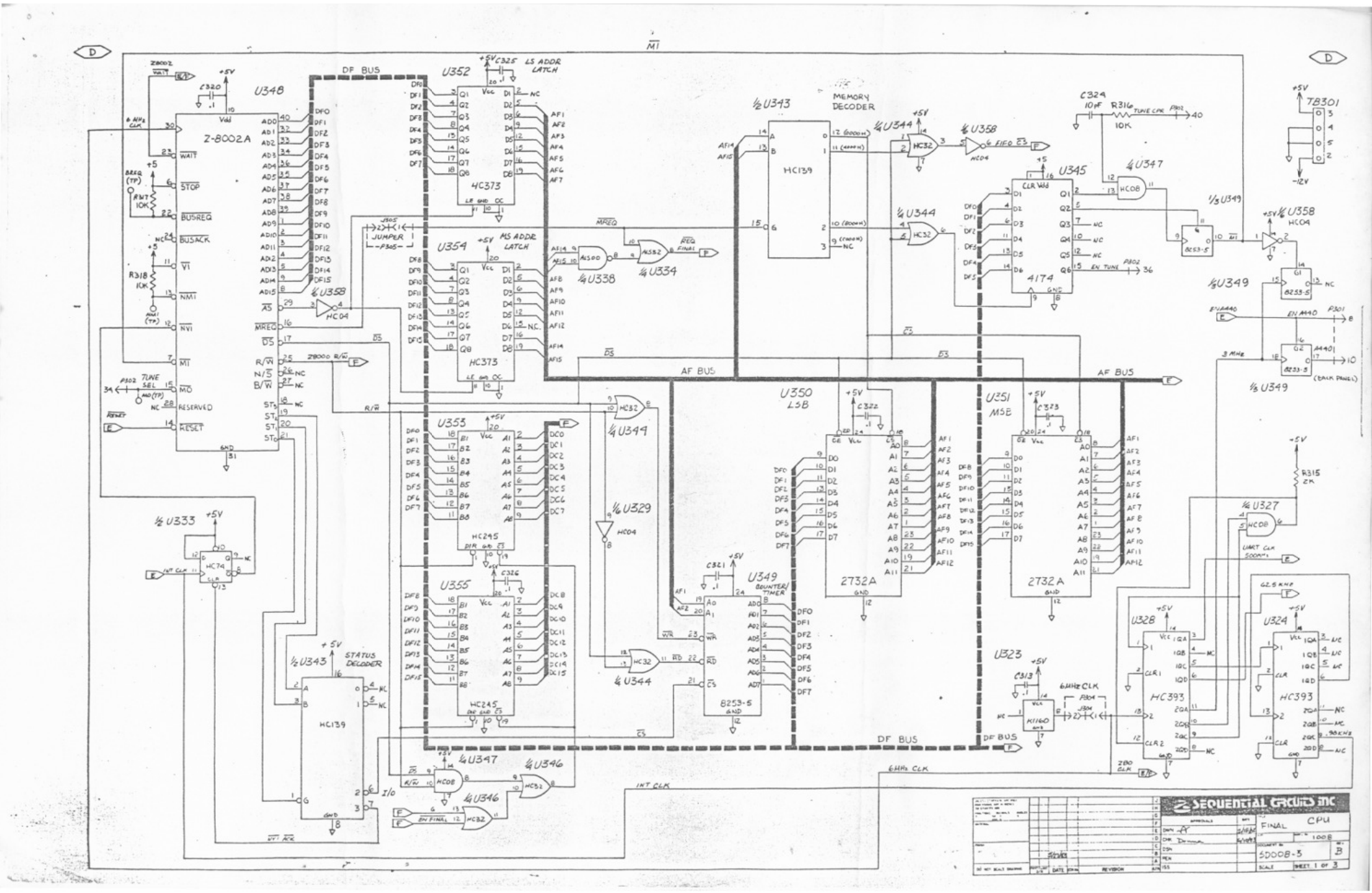
HARDWARE DESCRIPTION

FUNCTION		SCI PART #	PART DESCRIPTION
O.5.8		Washers	
		M-383	#4 STAR WASHER
		M-031	#6 STAR WASHER
		M-092	#8 SPLIT WASHER
		M-191	#8 STAR WASHER
O.5.9		Nuts	
		M-099	4-40 NUT 1/4" OD
		M-035	6-32 NUT 1/4" OD
		M-090	6-32 NUT
		M-091	8-32 NUT
	Control Mounting	M-152	POTENTIOMETER NUT
O.5.10		Cabling	
	Side Cable Clamps (4)	M-006	CABLE CLAMP
	Back Cable Clamp	M-088	CABLE CLAMP ADHESIVE
	Cable Ties (3)	M-140	3.5" TIE WRAP
		M-408	5" TIE WRAP
		M-151	1/4" SHRINK TUBING

454

O.H.2

Schematic D
SD008-3 1/3
50% reduction
11 X 17
Black line


Z-8002A
U348
DF BUS
U352
LS ADDR LATCH
U354
MS ADDR LATCH
MEMORY DECODER
½U343
HC139
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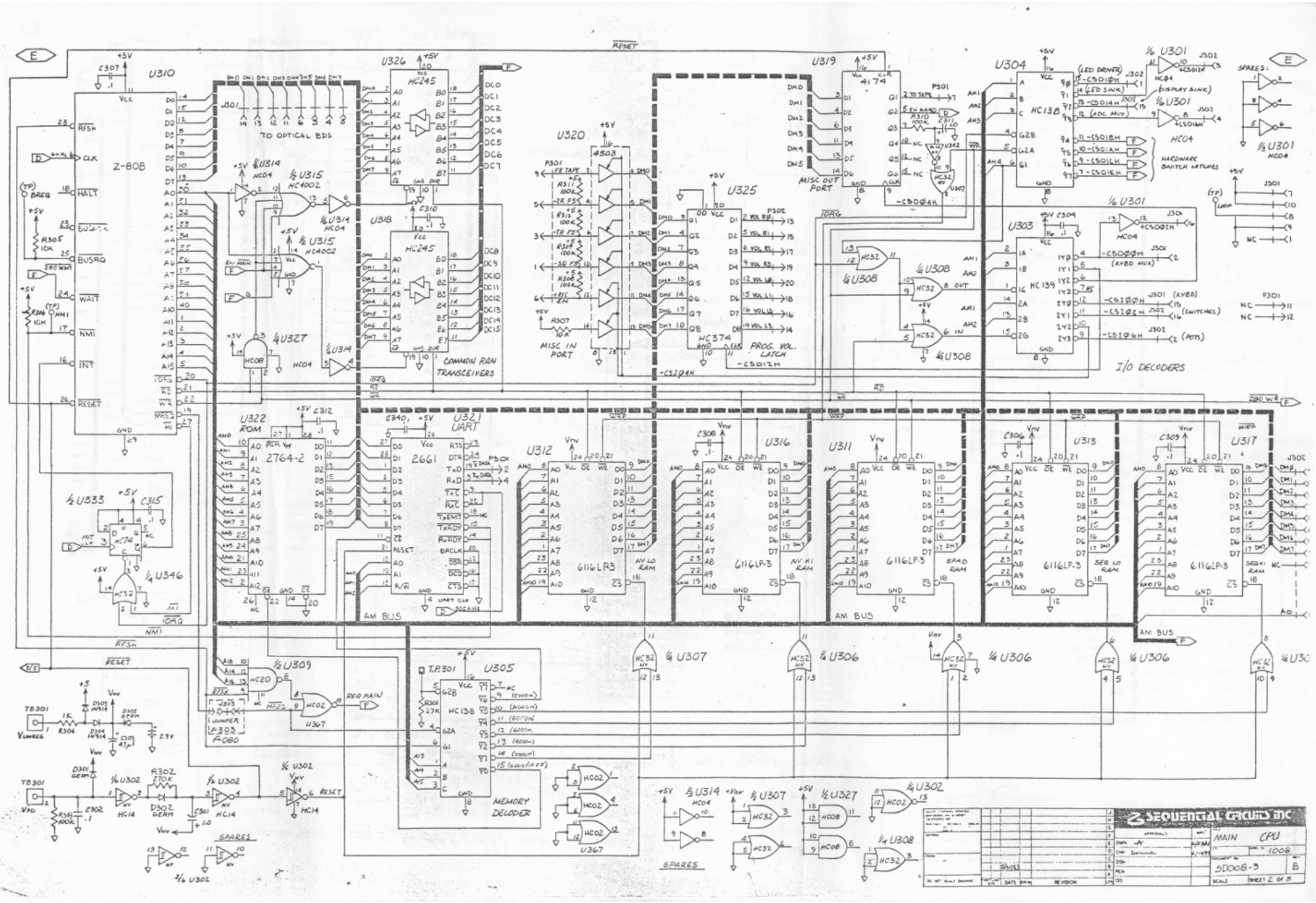
4174
U347
HC08
U358
HC04
U344
HC32
U338
AS00
U334
AS32
TB301
U350
LSB
U351
MSB
2732A
U349
COUNTER/TIMER
8253-5
U353
U355
HC245
HC373
U333
HC74
STATUS DECODER
U346
U327
U328
U324
HC393
AF BUS
6MHz CLK
INT CLK
SEQUENTIAL CIRCUITS INC
FINAL CPU
5D008-3
SHEET 1 OF 3

Schematic E
SD008-3 2/3
50% reduction
11 X 17
Black line


Z-80B
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TO OPTICAL BDS
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U320
4503
MISC IN PORT
U319
4174
MISC OUT PORT
U325
HC374
PROG. VOL. LATCH
U304
HC138
HARDWARE SWITCH LATCHES
U303
HC 139
I/O DECODERS
U322 ROM
2764-2
U321 UART
2661
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U316
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6116LP-3
NV LO RAM
NV HI RAM
SPAD RAM
SEQ LO RAM
SEQ HI RAM
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MEMORY DECODER
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SPARES
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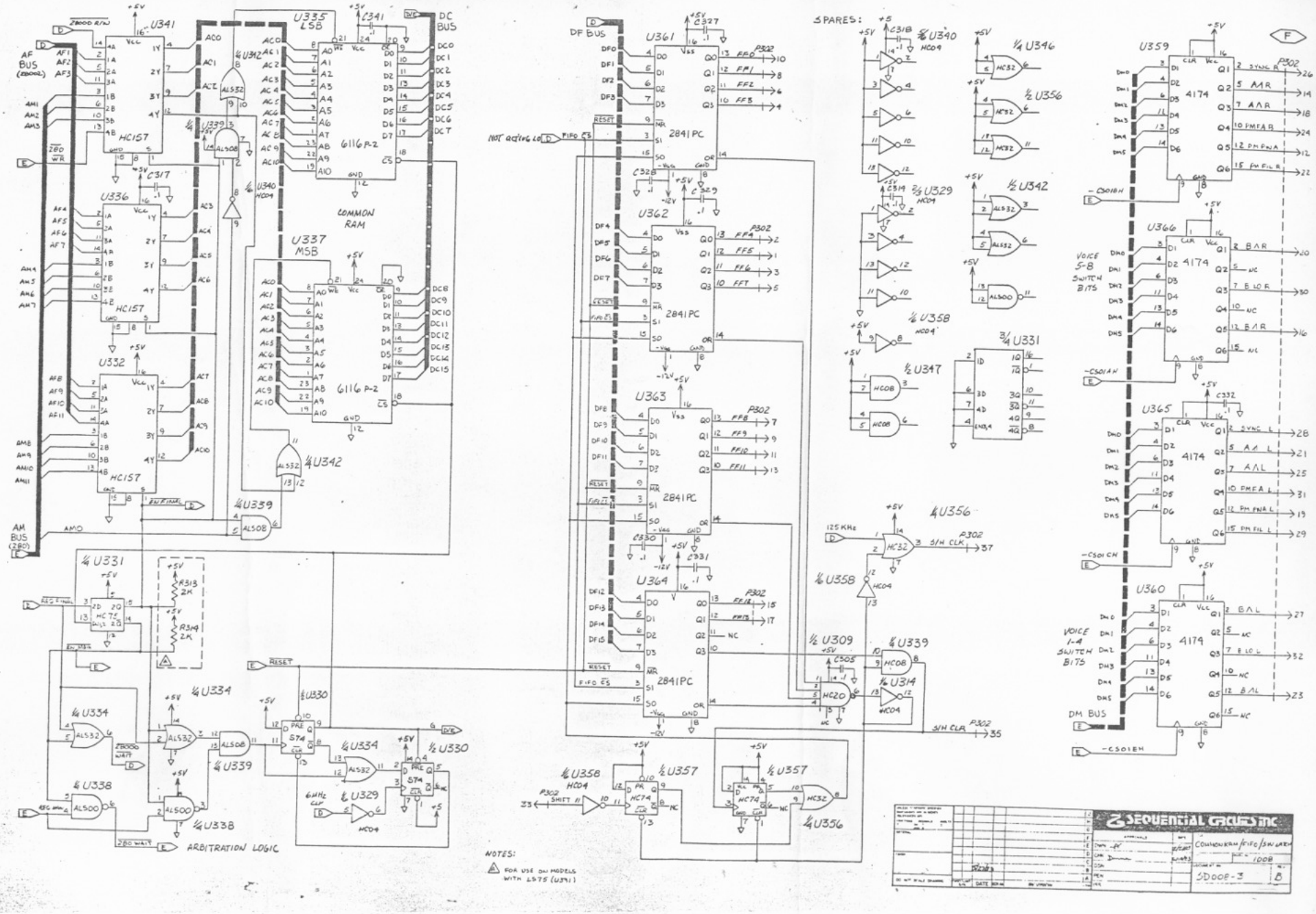
SEQUENTIAL CIRCUITS INC
MAIN CPU
100B
SD008-3
B
SHEET 2 OF 15

Schematic F
SD008-3 3/3
50% reduction
11 X 22
Black line


AF BUS (280002)
AM BUS (280)
DC BUS
DF BUS
U341
U335 LSB
U337 MSB
U336
U332
U361
U362
U363
U364
U359
U366
U365
U360
COMMON RAM
6116 P-2
2841 PC
4174
HC157
ALS32
ALS08
ALS00
HC74
S74
HC20
HC08
HC04
HC32
HC75
ARBITRATION LOGIC
SPARES:
VOICE 5-8 SWITCH BITS
VOICE 1-4 SWITCH BITS
DM BUS
125 KHz
NOTES:
FOR USE ON MODELS WITH 2575 (U391)
SEQUENTIAL CIRCUITS INC.
COMMON RAM/FIFO/SW ARCH
SD008-3
B

PCB 3 DESIG MAP
PP008-3
reduction 50%
11 X 22
2 color
Top layer black line/black screen
Bottom layer Blue screen

3.1 PROGRAMMER FUNCTIONAL TESTS

When power is switched on, LINK, PRESET, and RIGHT will be on.

3.1.1 RIGHT DISPLAY FUNCTIONAL TEST

1. To test the RIGHT PROGRAM display, select programs 11, 22, 33, ... 88 by pressing each PROGRAM/SEQUENCE switch twice.

   Note that switch #1 is lit. This indication is for the sequencer and is not relevant to program functions.

   Since LINK is on, as you select right programs, the left program numbers will change.
2. Test the right-side edit indicator by toggling any black-colored switch.

   The decimal point between the right digits lights.

3. Press PRESET.

   It should remain lit and turn the edit decimal off.

3.1.2 LEFT DISPLAY FUNCTIONAL TEST

1. Switch PROGRAMMER LEFT on.

2. To test the LEFT PROGRAM display, select programs 11, 22, 33, ... 88 by pressing each PROGRAM/SEQUENCE switch twice.

   Since LINK is on, as you select left programs, the right program numbers will change.
3. Test the left-side edit indicator by toggling any black-colored switch.

   The decimal point between the LEFT digits lights.
4. Press PRESET.

   It should remain lit and turn the edit decimal off.

5. Switch LINK MODE off. See that light goes out.

6. With LEFT on, select random programs to check that the right numbers don't change.

7. Switch RIGHT on. Again select some programs to check that the left numbers don't change.

3.1.3 RECORD MODE FUNCTIONAL TEST

1. On the back panel, switch RECORD to PROTECT (down).

2. On the control panel, press RECORD. It should not light.

3. On the back panel, switch RECORD to ENABLE (up).

4. Press TUNE to tune the -T8.

   You have to do this periodically as the instrument warms up. This will take from three to 20 seconds, depending on how far out of tune the oscillators are.

5. With LINK off, select SINGLE KEYBOARD.

6. Select a desired program on the RIGHT side.

   Play the keyboard. The notes will switch between left and right audio channels, according to which of the four left or right voices are assigned to the keys played.

   Note: Before proceeding, backup the owner's programs using the cassette interface if there is any doubt this has not been done. (See page O.17.)

7. Switch RECORD on.

8. Select LEFT.

9. Press any two PROGRAM/SEQUENCE switches.

   This records the RIGHT program into the LEFT location selected.

10. Verify that the RIGHT program is correctly recorded on the LEFT.

11. Now copy a LEFT program to the RIGHT.

12. Verify that it is correctly recorded.

15. To check the power on/reset circuit, rapidly switch power off and on a number of times. Check several programs to see if they have been altered.

Since you can't be familiar with everybody's programs, this test is best made with the Factory Programs.

3.1.4 MANUAL MODE FUNCTIONAL TEST

1. Switch PRESET off.

Entering manual mode removes programming from the synth so the sound produced is the result of however the switches and knobs happen to be set, rather than the program that is currently selected.

To set up a basic sound in manual mode, see the basic program diagram (page 4/5.9).

2. Switch PRESET back on.

3.2 SEQUENCER FUNCTIONAL TESTS

When power is switched on, PROGRAM/SEQUENCE switch 1 is lit.

3.2.1 BASIC RECORD/PLAY FUNCTIONAL TEST

1. Switch RECORD on.

   If it doesn't light, check that the back-panel RECORD switch is set to ENABLE.

2. Switch SEQUENCER SELECT/STOP on.

3. Press PROGRAM/SEQUENCE 1 (or other desired number).

4. Play some keys.

   The sequencer will start recording when and whatever you play, regardless of the keyboard mode (SINGLE, SPLIT, DOUBLE).

5. To stop recording, press SELECT/STOP.

   It will go off.

6. Switch SELECT/STOP back on.

7. Press PROGRAM/SEQUENCE 1 (or other number).

   The sequence will play back once, then stop. The sequencer remembers velocity but not pressure.

3.2.2 LOOP RECORD/PLAY FUNCTIONAL TEST

1. Switch RECORD on.

2. Switch SELECT/STOP on.

3. Press PROGRAM/SEQUENCE 2 (or other number).

   It will light.

4. Play something.

5. To stop recording, this time press RECORD.

The sequence will loop. SELECT/STOP will be lit.

3.2.3 RATE/PROGRAMMABLE RATE FUNCTIONAL TEST

1. Rotate the SEQUENCER RATE knob through its range.

This should change the playback speed of the loop.

2. Turn RATE to 4.

3. Press RECORD once.

RECORD will not light, but this records the value of the playback rate.

4. Switch SELECT/STOP off.

The sequence will stop.

5. Restart the sequence by switching on SELECT/STOP, then pressing PROGRAM/SELECT 2 (or other number).

The loop should play at maximum speed.

6. Center the RATE knob.

7. Press SELECT/STOP to stop playback.

3.2.4 FOOTSWITCH FUNCTIONAL TEST

1. Connect one of the footswitch outputs to the SEQUENCER FOOTSWITCH jack on the back panel.

2. Hold SELECT/STOP and press PROGRAM/SEQUENCE 1 (or other number).

The sequence will not start. This step "cues" the footswitch.

3. Press the footswitch.

The sequence will start.

4. Press the footswitch again.

The sequence will stop.

5. Switch RECORD on.

6. Switch SELECT/STOP on.

7. Select PROGRAM/SEQUENCE 2 (or other number).

8. Play something.

9. To stop recording, press the footswitch.

   The sequence will loop.

10. To stop playback, press the footswitch again.

3.2.5 ERASE FUNCTIONAL TEST

1. Erase all eight sequences and check that their LEDs work by repeating the following steps for each:

   a. RECORD on.
   b. SELECT/STOP on.
   c. PROGRAM/SEQUENCE.
   d. SELECT/STOP off.

2. Now check that the each sequence is actually erased by repeating the following steps for each.

   a. SELECT/STOP on.
   b. PROGRAM/SEQUENCE.

      Each time an erased sequence is selected, SELECT/STOP will go off after a moment.

3.3 MIDI FUNCTIONAL TEST

For a basic test of the transmitter and receiver circuitry, connect the -T8 to another MIDI synthesizer first as master (-T8 MIDI OUT to slave MIDI IN), then as slave (master MIDI OUT to -T8 MIDI IN. In both cases, playing the keyboard of the master should play notes on the slave. (According to the MIDI specification, all instruments are in Omni Mode on power-up, therefore there should be no problems with Mode or Channel selections.)

For more information on MIDI functions, refer to the SCI Prophet-T8 MIDIGUIDE (MG1008).

3.4 PRECAUTIONS BEFORE COMPUTER SERVICING

WARNING! You are responsible for the safe operation of this instrument under service conditions. Incorrect grounding practices can create lethal shocks. Scaling and other service operations must be performed with power on. Under these circumstances lethal voltage is present in the power supply primary area. Switch power off before disconnecting or connecting any circuitry, or removing or installing printed circuit boards (PCBs), integrated circuits (ICs), or other parts.

NOTE: Whenever the cover is removed, light may leak into the optical system and cause erratic operation. Always verify computer problems with the cover on.

NOTE: The diagnostics contain destructive memory tests. Before proceeding, be sure that the owner's custom programs are backed up on cassette. (If necessary, refer to page O.17.)

3.5 CHECKING SOFTWARE

Periodic refinements of the -T8's software occur to enhance features (such as MIDI) or correct minor problems which have revealed themselves only through extensive use.

Whenever any Sequential instrument is serviced, authorized service agents must check that its software is current. (Service agents find out the current software release by referring to the PROM Master List which is included with our Field Bulletins.)

Most -T8s left the factory with level 3_4. All should eventually be updated to level 3_4, which is current as of this writing. Level 3_6 adds a number of MIDI functions, and may be installed by authorized Sequential service centers. Details about level 3_4 and 3_6 software are available in the Sequential Prophet-T8 MIDIGUIDE (MG1008).

There may be more future releases. Owners staying abreast of their instruments may need to check their software level. The following procedure is provided especially for them. To check the current software level:

1. Switch power off.

2. Remove five screws each along the front and back edges of the top panel.

3. Lift off top panel (from back edge) and set it aside (where it won't get scratched!).

4. The Computer board (PCB 3) is on the left. The EPROM names are silk-screened on all but the earliest boards. The software level is written on the EPROM labels (see figure below).

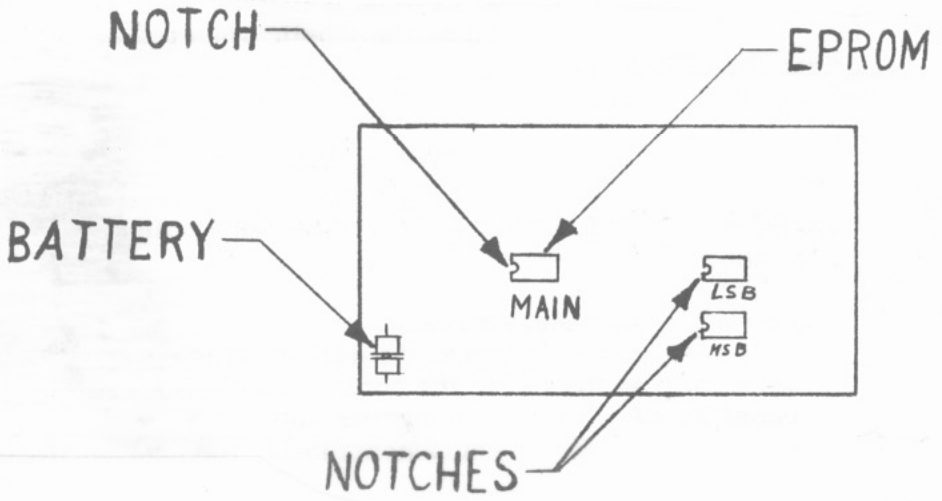


Figure 3.5
PCB 3 EPROM LOCATIONS

3.6 REPLACING SOFTWARE

You will presumably be receiving new software in a kit consisting of three EPROMs (Erase-Programmable Read Only Memories). They are embedded in conductive foam to nuetralize static charges. You don't need to be too paranoid about handling them in a normal, static-free environment.

One EPROM, marked "MAIN...," is a 28-pin type 2764 used in the 8-bit Z-80 computer. Two are 24-pin type 2732s, used in MSB (high byte) and LSB (low byte) positions in the 16-bit Z-8002 computer.

1. Switch power off.

2. Remove top panel.

3. Notice on the Computer board that all EPROMs are oriented so the pin 1 end "notch" is to the left. (See figure on previous page.)

4. Carefully remove the current MAIN EPROM. Because of the capacitor located between it and the adjacent RAM, you'll have to remove this chip by prying up the right side with a screwdriver. Don't bend the pins by prying up too sharply. Keep the screwdriver and EPROM parallel to the board while pulling upwards. Don't gouge the traces which run under the socket.

5. Remove the new MAIN EPROM from the foam, and put the old one there.

6. Inspect the pins of the new MAIN EPROM for straightness. Often, pins on new ICs tend to bend outwards and must be reshaped for an accurate mating to the socket.

7. Checking that the pin 1 end notch is oriented correctly, install the new MAIN EPROM. Before pressing down, make sure that all IC pins are correctly aligned to their sockets. Again, try to keep the IC parallel to the board.

8. Carefully remove the current FINAL MSB EPROM.

9. Install the new FINAL MSB EPROM.

10. Carefully remove the current FINAL LSB EPROM.

11. Install the new FINAL MSB EPROM.

12. Place the top panel back on (but don't install the screws until you test the instrument).

13. Switch power on and play a few programs. Changing software should have no effect on the programs and sequences stored in NV (non-volatile) memory. If some programs or sequences are changed, this may indicate a fragile PCB or intermittent computer problem. (In this case, see the Diagnostic procedures.)

14. Perform a full functional test of the instrument, including of course the new features documented in the software kit.

15. Return all three EPROMs to the factory for credit.

3.7 MAIN PROCESSOR (Z-80) DIAGNOSTICS

The Main (Z-80) computer system diagnostics are contained in the special "DT8-4" EPROM which is required to test the Z-80 system (order SCI #Z-1017.)

1. Switch power off.

2. Remove the top panel (see page O.20).

3. From PCB 3 (at the left) remove U322, MAIN ROM. (Observe cautions discussed on page 3.13)

4. Orient DT8-4 EPROM with end notch facing left, and install.

5. If Z-80 was disabled for Z-8002 test, unground the Z-80 BREQ test point. (Ignore this step if you have not yet run Z-8002 diagnostics.)

6. Disable Z-8002 by clipping the Final BREQ test point (located just above U348) to ground. There is a GND test point in the middle of the board.

7. Switch power on. The control panel will not light. The Main system is waiting for a bank of diagnostics to be selected. There are two banks of tests in the DT8-4 EPROM:

	Page
Bank 1 = MAIN computer system diagnostics	
M1 I/O port test	3.16
M2 LED test	1/2.11
M3 Local RAM test	3.17
M4 Common RAM test	3.17
M5 ADC test (pots, pressure sensors, wheels)	1/2.11, 10-14.7
Bank 2 = KEYBOARD tests for calibration and debugging	
K1 Test of unmounted optical system	7-9.11
K2 Single step test of key optics	7-9.10
K3 Looped scan of pressure sensors	10-14.8
K4 Single step test of pressure sensors	10-14.9
K5 Looped scan of optical system	7-9.9
K6 Pressure sensor slope analyzer test	10-24.10

8. Main is selected at first. After this, to select a MAIN test, you must first press the LEFT program switch, selecting Test Bank 1. The The LEFT and RIGHT displays will read "(blank) 1" and "1 1" respectively for four seconds. The displays will then go blank. Pressing PROG/SEQ switches 1-5 will then select MAIN tests M1-M5.

9. To select one of the KEYBOARD tests, you must first press the RIGHT program switch, selecting Test Bank 2. The LEFT and RIGHT displays will read "(blank) 2" and "2 2" respectively. The displays will then go blank. Pressing PROG/SEQ switches 1-6 will select KEYBOARD tests K1-K6.

10. The following tests are related to the Main processor: M1, M3, and M5. (Instructions for each test follow in this section.)

11. When done testing the Main processor, you can perform the Main I/O or Keyboard tests (listed above), or perform Final Computer diagnostics (see page 3.18), or return to normal operation.

12. When all diagnostics are concluded, to resume normal operation:

a. Switch power off and install the operating PROM.

b. Remove BREQ ground from Z-8002.

c. Switch power on. (If the Main Common RAM test was run, no programs will be heard because they have been erased. A-440 won't be heard because PROG VOLUME has been set to 0 in the Scratchpad.

d. Reinitialize the PITCH wheel (see page 1/2.6).

e. Reload programs (and sequences) through the cassette interface.

f. Because the test clears the Scratchpad, you must select both a program on the LEFT side and one on the RIGHT side. (This fills the Scratchpad from the Program memory.)

3.7.1 M1 I/O PORT DIAGNOSTIC TEST

For test setup instructions, see page 3.14.

If Bank 2 of the diagnostics has been selected prior to this test, press LEFT to select Bank 1.

Press PROGRAM/SEQUENCE 1.

When this test is selected, a blurry 88 will show in the RIGHT display. LINK, PRESET, RECORD, TUNE, SAVE, LOAD, LEFT and RIGHT will all be on (PRESET and LEFT will be somewhat duller than the others).

This test toggles each output port by alternatately writing 55H (0101 0101) and AAH (1010 1010) to it, and reads each input port. This verifies Chip Select decoding and latch functions.

When this test is selected, you should observe a square wave at each output of each latch in the Main system (see Figure 3.7.1.1). This verifies correct operation of the Output Port Decoding (Chip Selects). All input ports are being read (so if the -CSI is present, but the driver isn't operating normally, replace it).

Figure 3.7.1.1
I/O DIAGNOSTIC WAVE

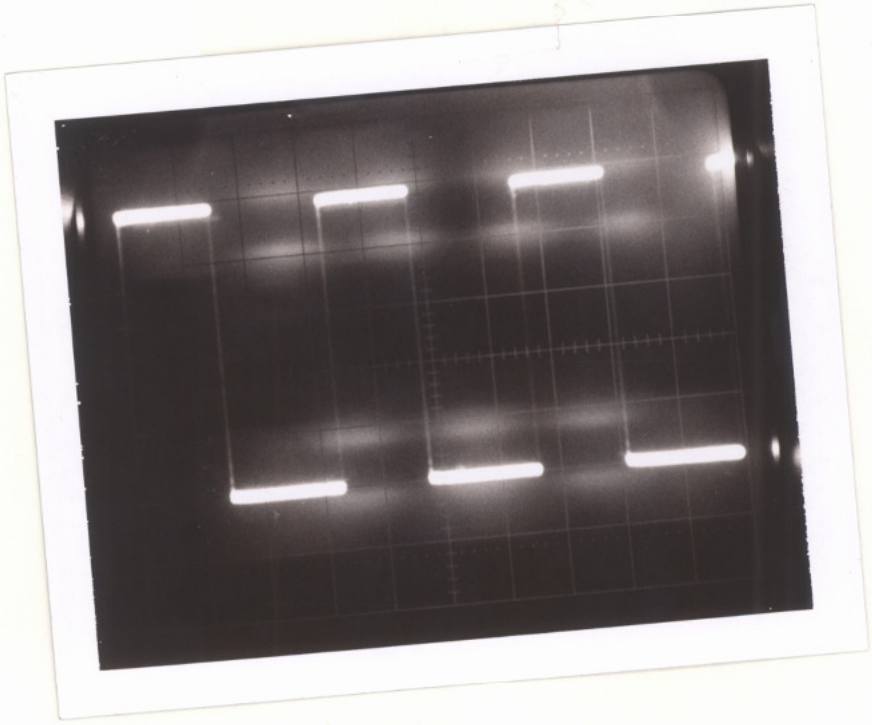


Figure 3.7.1.1

3.7.2 M3 MAIN RAM DIAGNOSTIC TEST

For test setup instructions, see page 3.14.

If Bank 2 of the diagnostics has been selected prior to this test, press LEFT to select Bank 1.

Press PROGRAM/SEQUENCE 3.

Continuously checks Scratchpad, Program, and Sequence RAMs. If the test is successful, only the (test) number "3" will be displayed. Otherwise, the PROGRAM/SEQUENCE LEDs will blink to indicate device failures as follows:

1	U312 failed
2	U316 failed
3	U311 failed
4	U313 failed
5	U317 failed

Note: Since **this test clears RAM,** to restore normal operation when done with diagnostics, you will have to reload programs through the cassette interface (see page O.19), and reinitialize the PITCH wheel (see page 1/2-6).

3.7.3 M4 COMMON RAM DIAGNOSTIC TEST

For test setup instructions, see page 3.14.

If Bank 2 of the diagnostics has been selected prior to this test, press LEFT to select Bank 1.

Press PROGRAM/SEQUENCE 4.

Checks the lower 1K of Common RAM. If the test is successful, only the (test) number "4" will be displayed. Otherwise, the PROGRAM/SEQUENCE LEDs will indicate device failures as follows:

1	U335 failed
2	U337 failed

(If the Z-8002 is accidentally not disabled, this will cause a false failure indication.)

3.8 FINAL COMPUTER (Z-8002) DIAGNOSTICS

These Z-8002 diagnostics reside within the standard operating system PROMs. There are three basic diagnostic tests plus fourteen tests which exercise each bit of the DAC. The tests are selected by momentarily (less than one second) grounding the Z-8002's NMI test point (located next to BREQ). Each ground tap advances to the next test. The only way to exit the routine is to reset by switching power off then back on. (If you unground the Z-80 BREQ, the -T8 will enter TUNE but not leave it.)

To activate Final diagnostics:

1. Switch power off.

2. If necessary, remove the top panel.

3. If Z-8002 was disabled for Z-80 test, unground the Z-8002 BREQ test point.

4. Disable the Z-80 by tying its BREQ (located just above U310) test point to ground. There is a GND test point in the center of the board. (With the Z-80 disabled, it doesn't matter which ROM--operation or DT8-4--is installed in the Main system. However for a complete check of Common RAM, the M4 test in Main Diagnostic EPROM DT8-4 must also be used--see page 3.17.)

5. Switch power on. As the Main processor is effectively disabled, the control switches won't work. Disregard any lit LEDs.

6. The Final system is now in a loop waiting for you to tap the Final NMI test point to ground, to select test #1. After doing this, wait for 5 seconds before looking at the MO waveform in test 1. These tests <u>are</u> consecutive.

FINAL COMPUTER (Z-8002) DIAGNOSTICS	
F1	MO TOGGLE (see page 3.19)
F2	COMMON RAM (see page 3.20)
F3	DAC (see page 4/5.34)
F4-17	BIT TESTS (see page 4/5.35-36)

7. Test 17 wraps around to test 1. To resume normal operation:

   a. Switch power off.

   b. Remove Final NMI grounding jumper.

   c. Remove Main BREQ ground from Z-80.

   d. If necessary, replace DT8-4 with standard Main operating ROM

   e. Switch power on.

   f. If necessary, reload programs (and sequences) through the cassette interface.

   g. To initialize Scratchpad, select programs in both Left and Right.

3.8.1 F1 MO (Micro Out) TOGGLE DIAGNOSTIC TEST

For test setup, see page 3.18.

This test activates a very short program to verify minimum Z-8002 operation, EPROM accessing, Final Data and Address busses, and power supply.

1. Connect scope to MO test point (to the right of BREQ).

2. You should see the following continuous pulse train. Otherwise indicates a basic failure in the Final system.:

Figure 3.8.1
MO (MICRO OUT) DIAGNOSTIC TEST

3. When done, select the Common RAM test by tapping the Final NMI to ground. This selects test F2.

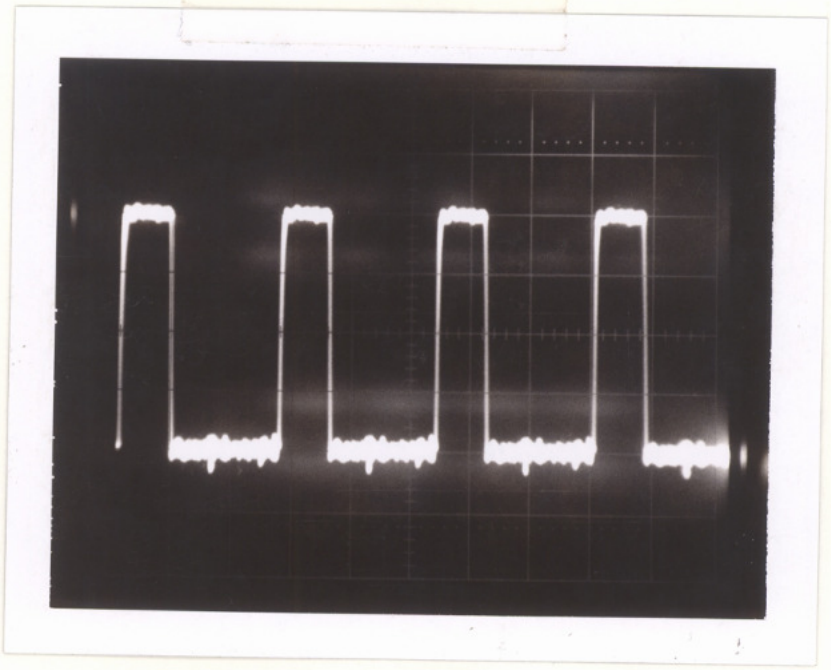


Figure 3.8.1

3.8.2 F2 COMMON RAM DIAGNOSTIC TEST

For test setup, see page 3.18.

Checks the upper half of Common RAM and associated arbitration logic.

1. Pass is indicated by a continuous train of widely-spaced pulses at MO:

Figure 3.8.2.1
FINAL COMMON RAM (GOOD)

V: 1V/div
H: 5ms/div

2. Fail is indicated by a high-frequency square wave:

Figure 3.8.2.2
FINAL COMMON RAM (BAD)

V: 1V/div
H: 2us/div

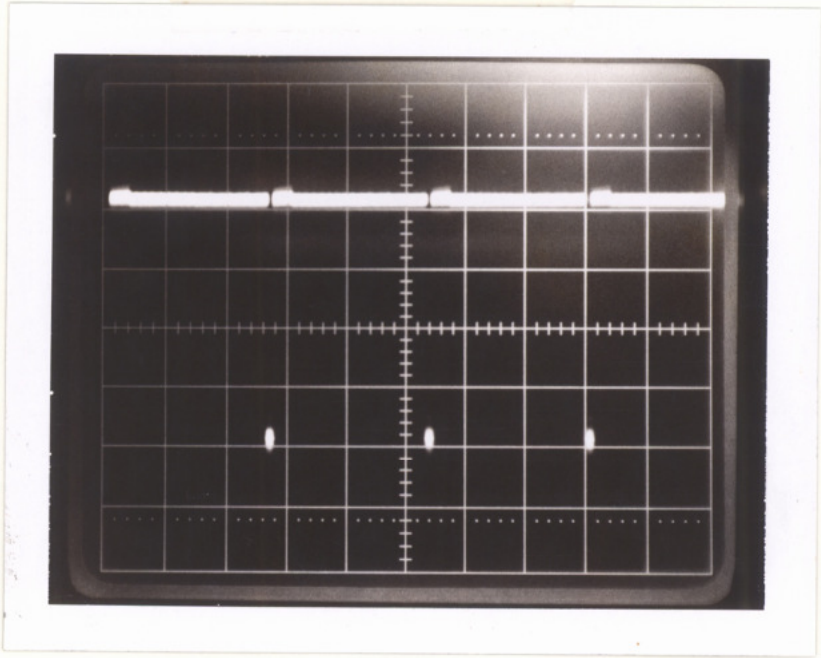


Figure 3.8.2.1

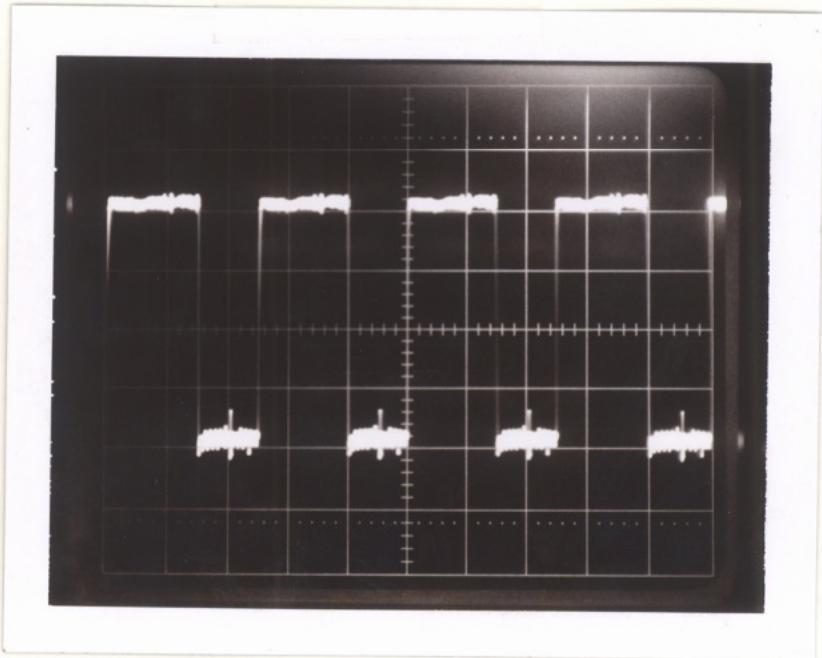


Figure 3.8.2.2

3. If waveform is correct, and the DT8-4 EPROM is currently installed in the Main system, temporarily enable the Z-80 by ungrounding its BREQ test point.

4. Press PROGRAM SELECT 4, which reactivates the Z-80 Common RAM test. The Main and Final Common RAM tests are now running simultaneously, which provides a 100% test of Common RAM circuitry. Pass is indicated by both the number "4" in the RIGHT PROGRAM display, and the waveform remaining as in Figure 3.8.2.1.

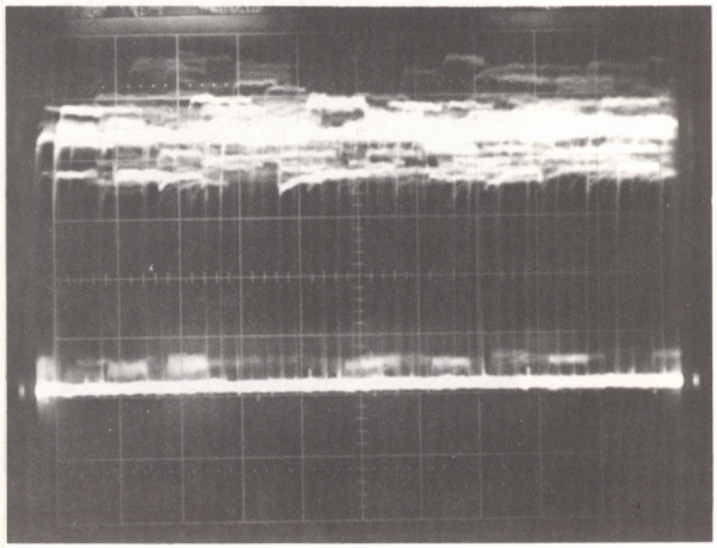
5. To continue with Final diagnostics, reground the Z-80 BREQ test point.

6. To advance to the next test, again tap the Final NMI test point to ground. (See page 4/5.34 for descriptions of remaining FINAL diagnostics F3-17.)

3.9 COMPUTER TROUBLESHOOTING

For troubleshooting, it should be emphasized that most computer malfunctions are caused by failures of devices connected to the data buss. A shorted latch input (for instance) can prevent an entire data line from achieving the minimum voltage needed to signify a high signal. Shorts between data lines will also confuse the computer terribly.

If you suspect a data buss problem, try to pick out the lines with questionable levels. For example, Figure 3.9.1 shows a normal data buss. The low voltages don't rise above 500 mV, while the high voltages are generally 4 to 5V, with occasional 3.5-V levels for CMOS devices. Note the solid ground line.

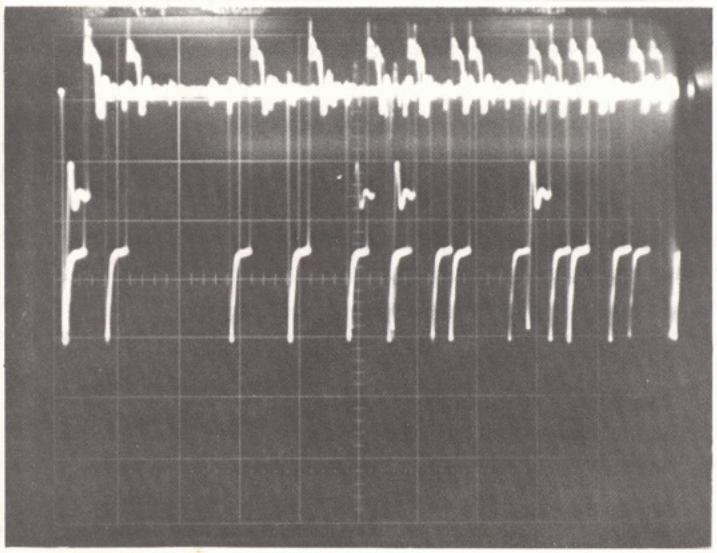


V: 1V/div
H: 1.9 us/div

Figure 3.9.1
NORMAL DATA BUSS

(over)

Figure 3.9.2 shows what the same buss line looks like when shorted to +5V by a failed device (in this case simulated by a 50-Ohm resistor.) The malfunction is indicated especially by the signals in the 1 to 3V range and by the lack of solid ground.



V: 1V/div
H: 1 us/div

Figure 3.9.2
SHORTED DATA BUS

Shorts may occur within a device or between printed traces. But since the computer is known to have been running, the problem is more likely to be device failure than a problem with the traces. Nevertheless it is probably best to begin troubleshooting the computer with a close visual inspection, especially around sockets. (Magnifying glasses are often helpful.) If you see no evidence of mechanical problems such as broken traces, broken sockets, conductive particles, botched soldering or careless repair attempts, try removing or swapping socketed devices such as the CPU, EPROM, and RAM. Even if the computer isn't running (due to one of these devices being missing), a change in static voltage indications could be a good clue about which is the bad part.

If you have checked all socketed components (perhaps even a few unsocketed ones), the best technique for finding a short is by making trace resistance measurements with a milliohmmeter. If you don't have such a sensitive ohmmeter, there may be no recourse but to cut printed circuit traces. The customary technique is to make the first cut at the electrical center of a the buss line, to isolate the problem to one half or the other. When the cut has yielded information on the direction of the malfunction, it should immediately be repaired--to prevent unrelated malfunctions. Then halve the suspect trace again, and so on, until the bad IC (or socket, or shorted trace) is isolated.

3.10 REMOVING PCB 3 COMPUTER

1. Raise boards (see page O.21).

2. To remove and replace PCB 3, refer to the following for the correct orientation of the connectors.

J301 (component side, upper left). Ribbon W4 passes over edge of board to PCB 9 at J901.

J302 (just under J301). Ribbon W2 connects to control panel, J101.

P301 (solder side, center). Unlike the others, ribbon W5 crosses under the middle of PCB 3, connecting to P602.

P302 (solder side, right). Ribbon W6 points away from the middle of PCB 3.

3.11 PCB 3 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-272	PCB 3 ASSEMBLED
		Z-282	PCB 3 POWER CABLE
		Z-1016	-T8 SOFTWARE SET

3.11.1 INTEGRATED CIRCUITS

U301-8,-10, -12 — Chip Select Inverters — I-249 — 74HC04 Hex Inverter

Three sections each reverse the polarity of an active-low chip select from the output port decoder. This is required to interface the clock inputs of the 4042, 4514, and 4515.

U302-2,-4,-6 — Power Detect/Reset — I-268 — 74HC14 Hex Schmitt Trigger

When power is off, battery BT301 provides Vnv, which powers U302. D305 drops Vnv to about 2.4V. Vnv also charges C301 and reverse-biases D301. Since the package is on and pin -1 is low, -2 is high. Through D302, this high on -3 makes -4 -RESET low (true). Likewise, pin 6 +RESET is true.

The Vpd input from the power supply is rectified dc--without filtering which would slow its edge. When power is turned on, it appears immediately. R303 completes a voltage divider (with R1507) which halves the value of Vpd. C302 is a filter. D301 requires Vpd/2 to exceed Vnv by about 400 millivolts before it can develop enough potential to toggle the first Schmitt trigger. So when power is switched on, -2 goes low after a brief delay. This begins to discharge C301 through R302.

Before this discharge is detected by the second Schmitt trigger, Vunreg from the power supply appears (as it was briefly delayed by C1501 charging). Passing through voltage-dropping resistor R304, it is clamped by D303 to not exceed about 5.4V. D304 brings this back down to +5V, which now overrides the battery supply. Vnv must be raised to 5V before the CPUs start-up, so the Non-Volatile RAMs are prepared to operate at full speed. C303 filters any spikes on the Vnv line. At this point D305 prevents Vunreg from charging BT301 (because lithium batteries are <u>not</u> rechargeable.)

So after Vunreg comes up, C301 discharges enough so -4 toggles, going high, which makes -RESET false. This frees-up the Main and Final processors to start, releases U319 Miscellaneous Output Port, and initalizes the Arbitration logic and the FIFOs. Then +RESET goes false, releasing the UART, and enabling the active-low RAM Chip Selects to be gated through the five decoder OR-gates U306/7.

When power is switched off, Vpd will fall rapidly, toggling both reset lines back to their true state. Of greatest importance, the RAM Chip Selects are disabled to prevent random instructions from being performed during power-down which could alter RAM contents. When Vunreg disappears, the battery supplies Vnv power.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U302-8	Write Protect	I-268	74HC14 Hex Scmitt Trigger

If the RECORD ENABLE/PROTECT switch on PCB 6 is set to PROTECT, the input -9 will be grounded. Any bit latched out of U319-7 will be shunted to grounded through R310 and D306. With input -9 low, -8 is high. U307-8 is therefore high, disabling all -WE (Write Enable) inputs on the NV RAMs.

When the RECORD switch is set to ENABLE, +REC EN is pulled high by R308. C311 therefore begins to charge through R310, as it is pulsed by the latch. The Schmitt Trigger detects this rise, toggling thus enabling U307-8 to gate the -WR signal to the RAMs.

U303 I/O Decoder I-254 74HC139 DUAL 2-4 DECODER

The first half generates output port chip selects to the keyboard multiplexer (U903-9), Programmable Volume Latch (U325-11), and miscellaneous output port (U319-9). The second half generates input port chip selects for the keyboard (U901/7-1,-15), switch matrix (U104-1,-19), miscellaneous input port, and pot and pressure sensor multiplexer (U108-16, U106-1,-19). The output defined by AM1/2 on the AB address inputs goes low when the G (gate) input goes low. These -OUT and -IN inputs are gated from the CPU's -IORQ, -WR, and -RD signals.

U304 Output Port Decoder I-253 74HC138 3 - 8 DECODER

Generates output port chip selects. The output defined by AM1-3 on address inputs ABC goes low when AM4 is high and both -IORQ and -WR are low. These chip selects clock latches on the control panel, and latches on this board, which control the analog switches in the synthesizer.

U305 Main Memory Decoder I-253 74HC138

Generates memory block chip selects. The Y output defined by AM13-15 on address inputs ABC goes low when -RFSH is high (at pin 6) and -MREQ is low (at pin 4). -RFSH indicates that the address buss holds a refresh address. You don't want to access memory while this is the case. -MREQ input indicates that the address buss holds a valid memory address. This is a condition required to access memory.

R301 satisfies -G2B. TP301 is for factory use. Tying it high disables memory access.

U306 RAM Write Protect I-251 74HC32 QUAD OR
U307-11

These gates are powered by Vnv. When power is off, RESET is high. So their outputs to the RAM chip selects are high, inhibiting any RAM activity (such as spurious write signals which can occur when power is switched off). When power is on, RESET goes low, enabling the active-low chip-selects.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U307-8 Write Protect I-251 74HC32 QUAD OR

If the back panel RECORD switch is set to PROTECT, U302-10 will be high. -8 will be high, disabling all -WE (Write Enable) inputs to the NV RAMs. When the RECORD switch is set to ENABLE, and U319-7 goes high, U302-8 goes low, enabling -WR signal from the CPU to the NV RAMs.

U308 I/O Decode Selector I-251 74HC32 QUAD OR

This logic gates three lines of the Control Buss, to enable either the Input or Output Decoder section of U303. If this is not an I/O operation, -IORQ will be high. -11 would be high, then -OUT and -IN high, or false. If on the other hand -IORQ is low, then AM4 must be low, or else again -OUT and -IN will be high. So, as long as -IORQ and AM4 are both low, -WR creates -OUT and -RD creates -IN.

U309-6 FIFO Ready I-250 74HC20 DUAL 4-IN NAND

When the FIFOs are empty of data, each OR (Output Ready) is low. -6 is high. U314-12, low. U358-12, high. This disables the S/H CLK from U356-3. Also U339-9 and -10 are low, so output -8 is low. This connects to the clock input of U357 Flip-Flop, and to the S/H Counter and Decoder on PCB 4.

When the FIFOs fill with data, the ORs go high. When they are all high, signifying that the first word is ready to be read, U309-6 goes low. This enables the S/H CLK to PCB 4. Input U339-9 is high, and it turns out that the most significant bit of the first word sent to the FIFO in each block move, is set, so U339-10 is high. U339-8 goes high. This clocks the flip-flop and writes the S/H CLR pulse to the S/H Counter and Decoder on PCB4. The pulse resets the counter and disables the decoder. After the first word in the FIFO is read, the MSB goes low, so U339-8 goes low, enabling the decoder.

U309-8 Main CRAM Request I-250 74HC20 DUAL 4-IN NAND

Pin 8 only goes low when -RFSH is false, and the three Address MSBs are high. If -MREQ is also low, REQ MAIN at U367-10 goes high.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U310	Main Processor (CPU)	I-055	Z-80B 8-BIT CPU

When power is off, the -RESET input is held low by U302-4. When power is switched on, the 6-MHz clock input (pin -6) starts up before -RESET goes high, which actually enables the CPU to start its program. D0-7 are the eight-bit Main Data buss (DM). All data flows to and from the processor over these lines.

Figure 3.11.1.1
DATA D0

V: 1V/div
H: .2 us/div

Figure 3.11.1.2
ADDRESS A0

V: 1V/div
H: .2 us/div

(over)

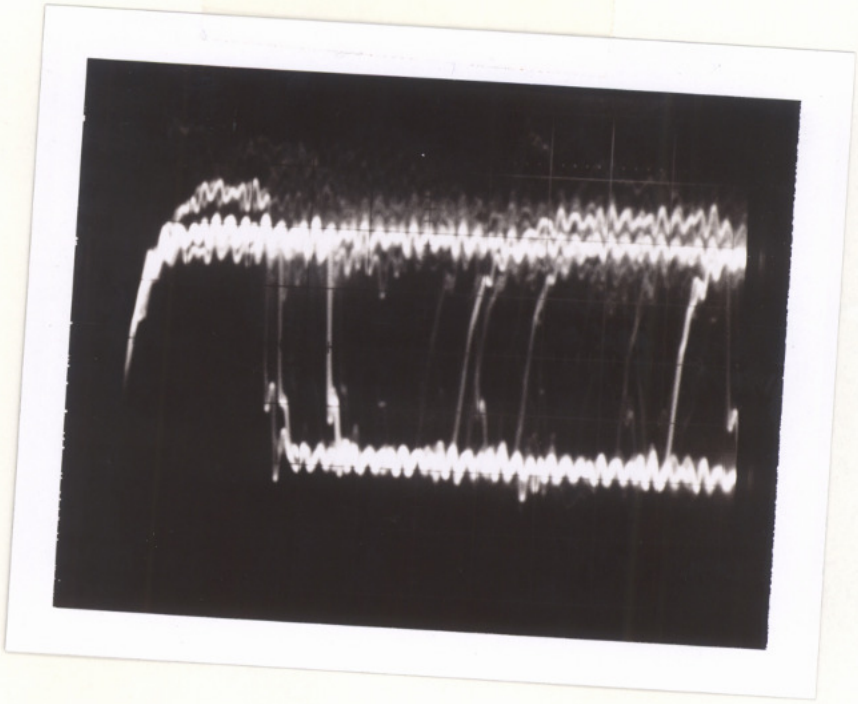


Figure 3.11.1.1

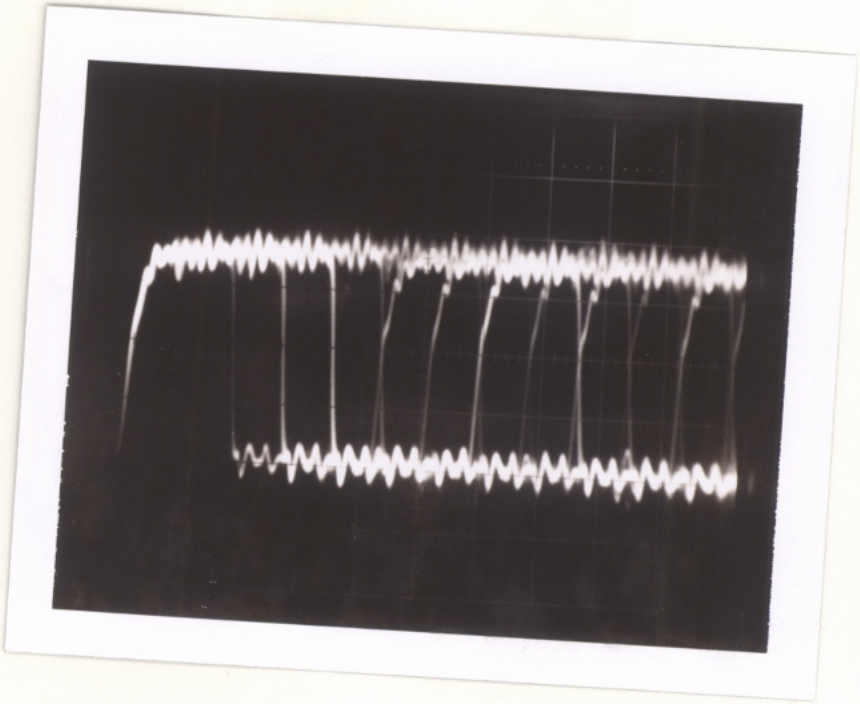


Figure 3.11.1.2

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U310, continued

When the -RD output is low, data on the buss is input from memory or an input port. This signal programs the direction of the Common RAM Transceivers, clocks data output from NV RAM, and gates the Input Port Decoder. When -WR is low, data on the buss is output to memory or one of the many output ports (latches). It enables the Scratchpad RAM, gates the Output Port Decoders and becomes a timing signal for the arbitration logic. (In Rev B of the PCB a jumper connects the -WR signal to U327-2).

A0-15 are the sixteen-bit address outputs from the CPU. This buss can identify either a memory, I/O, or refresh address, as indicated by -MREQ (pin -19), -IORQ (pin -20), or -RFSH (pin -28). Since it indicates that the address is for memory, the -MREQ output is used to enable memory chip selection (decoding). (The jumper shown across pins 1 and 2 of P303 allows insertion of factory test signals.) As a contrary indicator, -RFSH is used to inhibit memory decoding. Similarly to -MREQ, -IORQ enables the I/O port decoders.

-BREQ can be pulled low to disable the Z-80 while Z-8002 diagnostics are running. When the -WAIT input goes low, the CPU stops executing program instructions. The Arbitration Logic produces this signal, to inhibit the Main system.

The Z-80 has two interrupt inputs: -NMI (Non-Maskable Interrupt) and -INT (Maskable Interrupt). -NMI is normally pulled high by R306. In normal operation, when the UART receives a MIDI byte, or when it is ready to send one, either its -RxRDY or -TxRDY pull -NMI low. The CPU cannot ignore this signal. It immediately goes to the MIDI input subroutine which relieves the UART of its byte, so it can receive or transmit another one.

The 1-kHz (actually 0.98-kHz) interrupt clock is provided to both processors. The most critical processing activity, keyboard scanning, must be done at this rate to give sufficient resolution for velocity. Each low -INT pulse from the Interrupt Flip-Flop (INT FF) forces the Main processor into its Interrupt routine. (Actually because this interrupt is "maskable," there are some rare times when the CPU will ignore it.) First -M1 (a CPU cycle indicator) goes low, with -IORQ true causing a low -INT ACK (U346-3) which resets the FF. The INT FF has to be reset when first entering the interrupt state so the processor doesn't keep getting interrupted. The Main CPU then scans the entire keyboard. It scans the pressure sensors of keys which are down. (There is no reason to waste time scanning all the pressure sensors.) To prevent flickering, the front-panel LEDs are also strobed at this constant rate. The time between the end of interrupt processing and the appearance of the next interrupt leaves a "background" period for accomplishing less real-time dependent tasks such as control knob and switch reading, which therefore occurs over several interrupt cycles.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U311	Scratchpad RAM	I-511	6116LP-3 RAM 150 ns 2K x 8

This RAM earns its name as the CPU's work area, holding information about the status of the instrument, the control panel, and the keyboard. It is powered by Vnv, which is why, for example, you don't have to reinitialize the PITCH wheel every time power goes on. On the other hand, if this RAM is replaced, the PITCH wheel will have to be reinitialized.

To either read (-OE) or write (-WE), the 6000H memory block select must be gated through U306-3.

U312	PROG LO NV RAM 2000H	I-511	6116LP-3 RAM 150 ns 2K x 8
U313	SEQ LO NV RAM	I-511	6116LP-3 RAM 150 ns 2K x 8

8000H Non-volatile program and sequence memory. Similar to U311.

U314	Misc Inverters	I-249	74HC04

See U315 or U309-6.

U315	Common RAM Decoder	I-247	HC4002

This gate selects one of the two transceivers needed to interface the 8-bit Main Data buss to the 16-bit Common Data buss. To enable U318, AM0 must be low, -EN MAIN low, G low, and U327-3 low--which means that either -RD or -WR are low. Then U315-1 will be high and U314-4 low. Except that AM0 must be high (because of U314-2), U326 transceiver is selected in the same way.

U316	PROG HI NV RAM 4000H	I-511	6116LP-3 RAM 150 ns 2K x 8
U317	SEQ HI NV RAM	I-511	6116LP-3 RAM 150 ns 2K x 8

A000H Non-volatile program and sequence memory. Similar to U311.

U318	Main/Common XCVR	I-258	74HC245

Transfers MS byte data between the Main system and Common RAM. DIR input low (-RD) for input from Common RAM. -CE low when gated by U315-1, which is operated by the Arbitration Logic.

U319	Misc Output Port	I-228	4174 HEX LATCH

When power is off, RESET clears this latch to prevent spurious A-440 output or -WR pulses to NV. -CSO04 clocks it. TO TAPE receives some filtering on PCB 6 before going to the cassette deck. The EN A-440 bit follows the A-440 switch on the control panel. The third bit (pin 7) appears when the CPU wants to write to NV RAM. If the RECORD ENABLE switch is set to RECORD, C311 charges, which eventually toggles the Schmitt Trigger which enables the -WR line to the NV RAMs.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U320	Misc In Port	I-273	74HC367N HEX DRIVER

Early models used a 4503 here, which should be replaced.

When clocked by -CSI04, this drives cassette and footswitch data from the back panel, to the Main CPU. FR TAPE is a logic signal from the cassette comparator. Setting the back panel RECORD switch to PROTECT grounds pin 12, telling the computer to not allow the contents of the NV RAM to be altered. The RECORD LED will not light. The switch inputs are normally pulled high (active low).

U321 MIDI UART I-035 2651 (2661) USART

The UART has two control registers that are accessed as memory locations. While playing, the UART always transmits. The transmission occurs at 31.25 kBaud, which is obtained by internally dividing the 500 kHz TxC (and RxC) input by 16. The UART appears as memory block C000H to the decoder. AM0 and AM1 select the registers, while AM2 defines the read or write address.

C000H	Received data register
C001	UART status register
C003	Read UART command register
C004	Transmit data register
C006	Write UART mode register
C007	Write UART command register

The UART converts parallel bytes written to its memory-mapped transmit register into serially-formatted bytes consisting of a start bit, 8 data bits (D0 to D7), and a stop bit. The output goes to the MIDI drive gate on PCB 6.

RxD connects to the MIDI IN optoisolator. When the UART has not received data, its pin 14, -RxRDY is high. But when a complete serial byte is received, -RxRDY goes low, indicating the receive register is now holding data. This data needs to be retrieved, so that the next byte of data can be received. When it sees this negative edge on its pin 17, the CPU branches to the routine which handles the UART input.

U322 MAIN EPROM Z-1013 8 Kbyte EPROM (2764-2)

Version 3-4 or above.

The ROM is the lowest memory-mapped device. Decoder output 0000/1FFFH enables the output of the EPROM (-OE). The EPROM places the program instruction on the data buss (DM0-DM7), from which it is retrieved to the CPU's instruction register. (Although using the 2764 -CE input would reduce power consumption, -OE was used for maximum memory access speed.)

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U323 System Clock I-508 6 MHz MODULE

Output from the 6-MHz clock module is jumped through a connector to allow the substitution of test clocks at the factory. It goes to the clock input of both processors, to the Arbitration Logic, and to divider U328.

U324 Interrupt Divider I-261 74HC393 Dual 4-BIT COUNTER

Divides 125 KHz input to .98 kHz -INT CLK output which goes to the Interrupt Flip-Flops in both the Main and Final systems.

U325 Programmed VOL Latch I-260 74HC374

When clocked by -CSO02H, this latches four bits each for the Left and Right Digitally-Controlled Attenuators on PCB 6.

U326 Main/Common LS XCVR I-258 74HC245

Transfers data between the Main system and Common RAM. DIR input low (-RD) for input from Common RAM. -CE low when gated by U315-13, which is operated by the Arbitration Logic and inverted by U314-6.

U327 Misc Logic I-262 74HC08 QUAD AND

See U315 or U328.

U328 Clock Divider I-261 74HC393 Dual 4-BIT COUNTER

Input is 6 MHz. Pin 11 supplies 3 MHz to the A-440 and Tune circuitry. U327-6 resets section 2 of the counter to produce 1 MHz at pin 9 (rather than 0.75 MHz) which clocks section 1 to produce 500 kHz to the UART, 125 kHz to U324, and 62.5 kHz, which clocks the S/H decode logic.

U329 Misc Logic I-249 74HC04 HEX INVERTER

See U344 or U330.

U330 Arbitration Logic FF I-057 74S74

The function of Arbitration logic is to produce the G (Gate) signal which, when low, enables Common RAM.

When power is off, -RESET (U330-10) is low. When power appears, there is an instant during which U330 is energized, but -RESET is still low. This low presets the Q output, pin 9. This high G signal does several things. First, it inhibits access to Common RAM. Second, it enables U331-15 to transfer the -REQ FINAL signal into the Arbitration Logic. Third, it inhibits both the Final and Main Transceivers to Common RAM.

(over)

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U330, continued

During normal operation, -RESET is high. G is normally high unless a low is detected at U330-13, generated by U330-5. U330-5 is normally high unless pin 2 is low, which will only occur when U330-8 and U339-11 are low as a result of either computer system requesting Common RAM (see U331-15). The 6MHz clock (inverted by U329-6) then gates the low level at U330-2 to pin 5, enabling the clear input at U330-13, making G go low, presetting U330-5 again, removing the clear enable. G will only go high again when U339-11 goes high as a result of the request coming to an end.

U331-15 Request Enable FF I-510 74HC75 4-BIT COUNTER

When neither system is requesting Common RAM, -REQ FINAL is high. Input pin -2 of U334 is high. Output U334-3 is high. The -EN FINAL output from U331-15 is high because pins 3 and 13 are high. This is applied to gate inputs U334-1 and U338-1. Since REQ MAIN to U338-2 is low, output U338-3 is high. With highs on both its inputs, U339-11 is high.

Returning to U331, pin -14 is low. (R313/14 interface the HC logic family to ALS.) But U334-4 is high, so U334-6 is high. In other words, the -Z8000 WAIT signal is false and the Final CPU goes about its business. Also, since U338-4 is low, U338-6 is high, enabling the Main CPU do the same.

When -REQ FINAL goes low, U334-4 and -2 go low instantly. Since the G signal from U330-9 is high, -REQ FINAL then appears true at pin -15, -EN FINAL. When this low hits U334-1, U334-3 goes low. So U339-11 goes low. -EN FINAL also brings U338-1 low, so U338-3 remains high.

Looking again at U331, since -15 is low, -14 is high, so -EN MAIN is false. Since U334-5 is high, -Z8000 WAIT stays high (inactive). If REQ MAIN occurs while -EN MAIN is inactive, these two highs make U338-6 go low, which tells the Main CPU to wait.

When -REQ FINAL goes high (false), U334-6 is high (-Z8000 WAIT false), and U334-2 and -3 go high. U339-11 goes high, clocking the input of U330. G enables U331-15 (-EN FINAL) to go high. U331-14 goes low (-EN MAIN true), inhibiting the -Z80 WAIT signal at U338-6. When REQ MAIN appears, U338-3 goes low, forcing U339-11 to return low, forcing G low, inhibiting any -REQ FINAL from activating arbitration logic (-Z8000 WAIT would go true instead), until the MAIN REQUEST is finished.

U332 Common Address Select I-255 74HC157

In parallel with U336 and U341, this allows either the Main (B inputs) or Final (A inputs) Address busses to define a location in Common RAM (Y outputs). The Main system writes to Common RAM more often than the Final reads from it. Therefore the Final Address buss is only selected when -EN FINAL is low.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U333-6	Main Interrupt Flip-Flop	I-252	74HC74

The INT CLK input is a constant .98-kHz clock. When it goes high, -Q goes low, interrupting the Main CPU. When responding to an interrupt, the CPU generates an -IORQ with -M1 low, clearing the FF through U346-3 (-Q returns high). For more information on interrupts, see U310.

U333-8	Final Interrupt Flip-Flop	I-252	74HC74

The INT CLK input is a constant .98-kHz clock. When it goes high, -Q goes low, interrupting the Final CPU. The -NVI ACK which clears the FF is produced automatically by the Status Decoder. For more information on interrupts, see U348.

U334-3, -6, -11	Arbitration Logic	I-054	74ALS32

See U330 or U331.

U334-8	REQ FINAL Logic	I-054	74ALS32

Produces -REQ FINAL when Final -MREQ is low, and AF14/15 are low (U338-8). -REQ FINAL goes to the Arbitration Logic.

U335	Common RAM LSB	I-512	6116P-2 RAM 120 ns 2K x 8

The Common RAM holds output from the Main system (as block E000H), for use by the Final system (to which it appears as block C000H). Therefore the data input/outputs connect to both the Main and Final transceivers. The Address inputs come from either the Main or Final system, as determined by the Address buss selectors (U332, U336 and U341). To either write or read, -CS (G) must be low. Write is programmed by the -WE input. When this is high, the memory access is a read.

U336	Common Address Select	I-255	74HC157

Similar to U332.

U337	Common RAM MSB	I-512	6116P-2 RAM 120 ns 2K x 8

Similar to U335.

U338	Misc Logic	I-052	74ALS00

See U331-15 or U334-8.

U339	Misc Logic	I-053	74ALS08

See U342, U331-15, or U309-6

U340	Misc Logic	I-249	74HC04

See U342.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U341	Common Address Select	I-255	74HC157

Similar to U332. Notice that along with the AM or AF 1, 2 and 3, U341 also passes the Z-80 -WR or Z-8002 RD/-WR lines through output 4Y.

U342 — Common RAM Select — I-054 — 74ALS32

To write to one of the Common RAMS, its -WE must go low. For the LS RAM, this occurs when the Z80 or Z8002 -WR signal from U341-12 is low, and U339-3 is low. This will be true unless both -EN FINAL is false (high) and AM0 is a 0. For the MS RAM, there must also be one of the CPU -WR signals, and either -EN FINAL or AM0 must be low.

U343-4 — Status Decoder — I-254 — 74HC139

The ST Status outputs from the Z-8002 decode up to 16 different processor states. When ST0 and ST2 are low and ST1 is high, output pin -6 goes low. This generates the single I/O select which allows writing to and reading from U349 Timer/Counter. Pin -7 goes low when ST0 is low and ST1 and ST2 are high. This low clears U333-8 NVI FF.

U343-12 — Final Memory Decoder — I-254 — 74HC139

When the Final computer generates a low on -MREQ, AF14 and AF15 select the operating program, FIFO buffer, or (memory-mapped) Tune Control Latch.

U344-3, -6 — Memory Strobe — I-251 — 74HC32

-FIFO CS (U358-6) will be true when the Memory decoder produces the 4000H enable. The 8000H signal will clock U345 Tune Latch. -DS is generated by the processor to synchronize the transfer of data.

U344-8, -11 — Timer Strobe — I-251 — 74HC32

-WR to the Timer will be true when R/-W is low, and -DS is low. -RD will be true when R/-W is high through U329-8, and -DS is low.

U345 — Tune Control Latch — I-513 — 74HC174

The Tune latch is memory-mapped (8000H) for maximum speed. Normally the EN TUNE bit will be low, to disable the output of the Tune Comparator on PCB 5. (The EN TUNE bit goes to PCB 5 via PCB 4.) When EN TUNE goes high, the comparator output is enabled, and appears, through filter R316/C324, at U347-12. The Q1 bit is used to gate the TUNE CPR signal to the Cycle Counter. The Q2 bit enables (gates) the Cycle Counter.

U346 — Misc Logic — I-251 — 74HC32

See U333-6 or U353.

-ESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U347	Misc Logic See U345 or U353.	I-262	74HC08
U348	Final CPU	I-047	Z8002A 16-BIT CPU

When power is off, the -RESET input is held low by U302-4. When power is switched on, the 6-MHz clock input (pin -30) starts up before -RESET goes high, which actually enables the CPU to start its program. AD0-15 form a multiplexed Address/Data buss. When the AD buss is data, output -DS (Data Strobe) goes low. When the buss holds an address, this is indicated by the -AS (Address Strobe) output. This signal (inverted at U358-4) clocks two latches (U352 and U354) which transfer the CPU Address to the Final Address Buss.

Figure 3.11.1.3
AD0/DF0

V: 1V/div
H: .2 us/div

When R/-W output is high, data on the buss is input from memory or an input port. When R/-W is low, data on the buss is output to memory or one of the output ports (latches). This signal programs the direction of the Common RAM Transceivers, enables writing to Common RAM, and determines the direction of counter/timer transfers.

Since it indicates that the address is for memory, the -MREQ output is used to enable memory chip selection (decoding). (The jumper shown allows insertion of factory test signals.) -MREQ also gives rise to the -REQ FINAL signal.

(over)

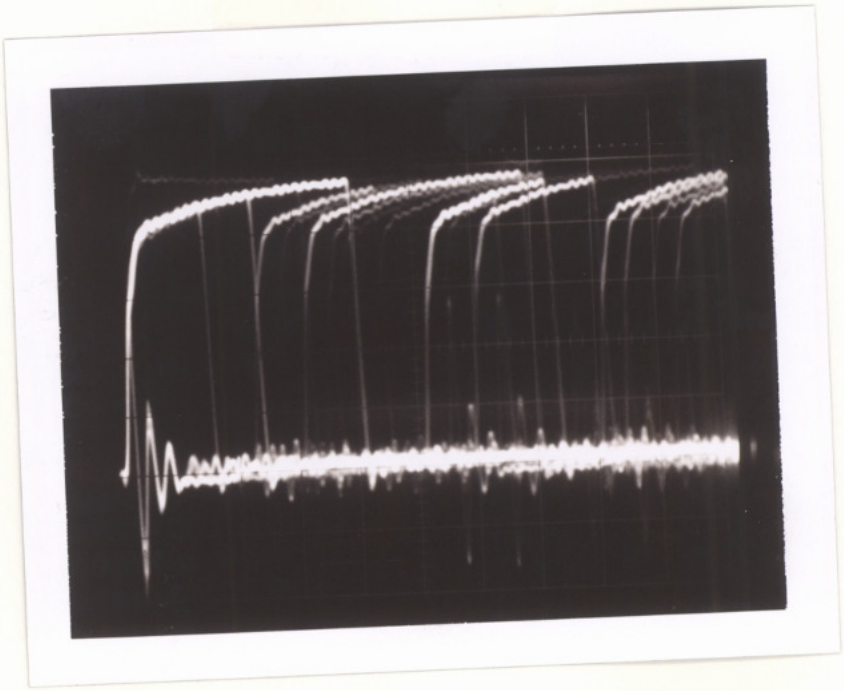


Figure 3.11.1.3

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U348, continued

-BREQ can be pulled low to disable the Z-8002 while Z-80 diagnostics are running. When the -WAIT input goes low, the CPU stops executing program instructions. The Arbitration Logic produces this signal, to inhibit the Final system if it requests Common RAM while the Main system has been granted access to it.

The Z-8002 has three interrupt inputs: -NMI (Non-Maskable Interrupt), -VI (Vectored Interrupt), and -NVI (Non-Vectored Interrupt). -VI isn't used. -NMI is normally pulled high by R318. TP304 is used to momentarily ground -NMI to select Final diagnostics.

The Final processor is interrupt-driven because it must perform the real-time task of velocity and envelope calculation. It counts -NVI interrupts and clears them with the -NVI ACK signal from the Status Decoder. It responds only to every third clock, with the same routine for CV output and calculation. This gives the envelopes a basic resolution of 3 milliseconds (actually, 3 x .98 kHz = 2.94 ms, but who's counting?).

During the TUNE routine, -MI (Micro In) monitors the Cycle Counter. That output, U349-10, goes low after each period of oscillator (or filter) measurement. MO (Micro Out) is used to toggle the Left/Right TUNE selector on PCB 5 (0=L, 1=R). MO goes to PCB 5 via PCB 4.

U349 Counter/Timer I-414 8253 TIMER (TIGHT SPEC).
Do not use I-051 (8253 loose spec).

This chip serves both the A-440 and TUNE circuits. This is a three-section device, with a control register and three counter registers which can be read to or written from.

0006H	Mode Set
0000	Counter 0, One-Shot
0002	Counter 1, Tune Timer
0004	Counter 2, A-440

The major section of U349 drawn in the lower center of sheet D shows the Data buss connections which transfer data between the processor and U349's registers, the address connections which select the registers, and the control signals which select the chip and define -WR or -RD.

When EN A440 (U319-5) goes high, it gates the third section to divide the 3 MHz clock input to an A-440 square wave at pin -17. Both this enable signal and the A-440 product go the Audio Output circuitry on PCB 6.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U349, continued

Looking now at TUNE CPR, the squared-up oscillator or filter pulses from the Tune Comparator are gated by U347-11, which clocks input pin -9. When the Cycle Counter is enabled by a high on pin 11, its output pin -10 goes low of the first edge of the clock. -MI notifies the CPU of this occurence. U358-2 inverts the low into a high which gates the Total Time Counter. This Total Time Counter now begins to accumulate a number of 3-MHz pulses. When the Cycle Counter has accumulated a specific number of cycles (which are programmed for each octave), its output goes high. This becomes a low which stops the Total Time Counter. The Total Time Counter then holds the number of 3-MHz pulses which occured during the programmed number of cycles. Each pulse counts 1/3 microsecond. Therefore, for example, if the Cycle Counter was programmed for one cycle and the Total Time Counter now equals 11,494 the input frequency is 261 Hz. (1/3 us x 11,494 = 3.83 ms indicating 261 Hz)

U350	Version 3_4	Z-1014	FINAL LSB EPROM (2732A)
U351	Version 3_4	Z-1015	FINAL MSB EPROM (2732A)

U348 Final Processor reads a word from U350 and U351 EPROMs by decoding a Chip Select through U343-12, when -MREQ is true. Program instructions are placed on the buss when -DS is true. For information on software versions see the Operation Manual or the latest MIDIGUIDE.

U352	Final LS Address Latch	I-259	74HC373

Latches the Final Address, when -AS is low (U358-4 high).

Figure 3.11.1.4
ADDRESS AF1

V: 2V/div
H: .2 us/div

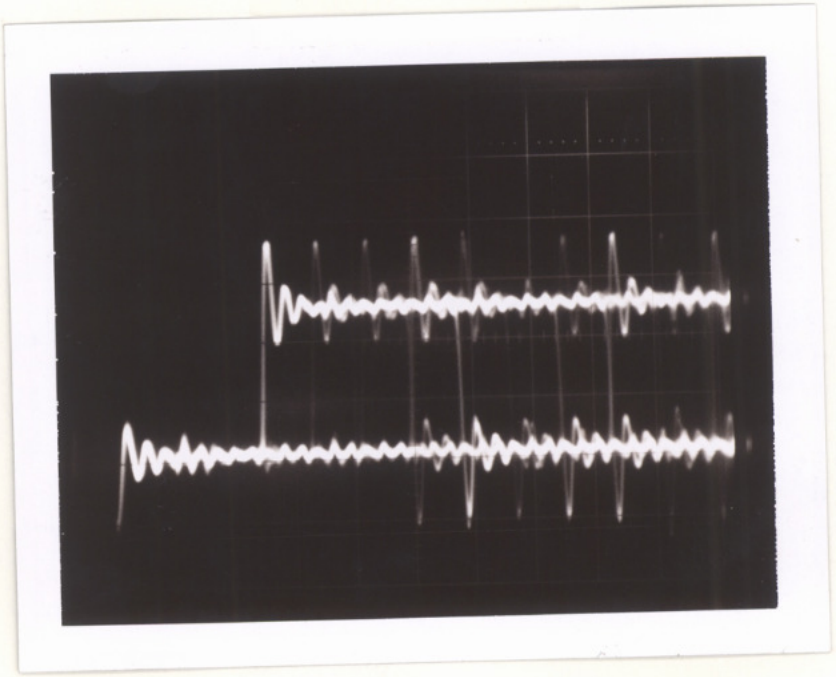


Figure 3.11.1.4

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U353	Common/Final LS Xcvr	I-258	74HC245

U353/355 are enabled by U346-8 when -EN FINAL and G are low (U346-11) and U347-8 is low, which it will always be when -DS (Data Strobe) or R/-W are low. The direction of the data is determined by R/-W.

U354 — Final MS Address Latch — I-259 — 74HC373
Similar to U352.

U355 — Common/Final MS xcvr — I-258 — 74HC245
Similar to U353.

U356 — Misc Logic — I-251 — 74HC32
See U309 or U357.

U357 — FIFO Scan Logic — I-252 — 74HC74
When the FIFOs are empty of data, each OR (Output Ready) will be low. U309-6 will be high. U314-12, low. This clears both FF sections.

When the first data word (FFH) "falls-through" the shift registers and arrives at the output, the ORs go high. When they are all high, signifying that the first word is ready to be read, U309-6 goes low. U314-12 goes high. Input U339-9 is high. Because the most significant bit of the first word in the FIFO is set, U339-10 is high, so U339-8 goes high. This clocks U357-3, so pin -5 goes high and clocks S0 on all the FIFOs. This also forms the S/H Clear signal which resets U450 S/H Counter, and inhibits U457 S/H Decoder. This synchronizes reading data from the FIFOs, through the DAC, to the sample/holds.

When monitoring Vdac with a scope, you will see each cycle start with a brief, full-scale spike. This is the FFH code word which starts each DAC cycle. Just after U450 is reset, data is clocked out of the FIFO at a constant and much slower rate.

When SHIFT goes low, the high from U358-10 clocks out a high from U357-9. This is the principle shift signal which activates the FIFO S0 inputs. After each shift pulse, OR goes false while the FIFO outputs stabilize, clearing the shift FF's.

U358 — Misc Logic — I-249 — 74HC04
See U349, U352, U344, U357, or U309.

U359/60 — Synth Switch Latches — I-228 — 4174 HEX LATCH
Output switch bits control analog switches in the Left or Right Synthesizers. Pin 9 receives a chip select from U304, then strobes data from the Main data buss.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U361-64	FIFO Buffer	I-050	3341 FIFO

First-In-First-Out is the order in which at the beginning of each interrupt cycle, the Final CPU does a high-speed block move of 59 sixteen-bit words to this buffer memory (memory-mapped at 4000H). Output Ready (OR) goes high. The processor continues with other tasks while the timing logic synchronizes reading the FIFO output to the DAC and Demultiplexer.

When power is off, -RESET clears the FIFOs so no spurious words are spoken to the DAC. The -FIFO CS comes from the Final Memory Decoder. The FIFO Scan Output (SO), which writes the next word to the output register is clocked either by the S/H CLR signal (through U357-5) or (U356-8) the inverted SHIFT signal from U357-9.

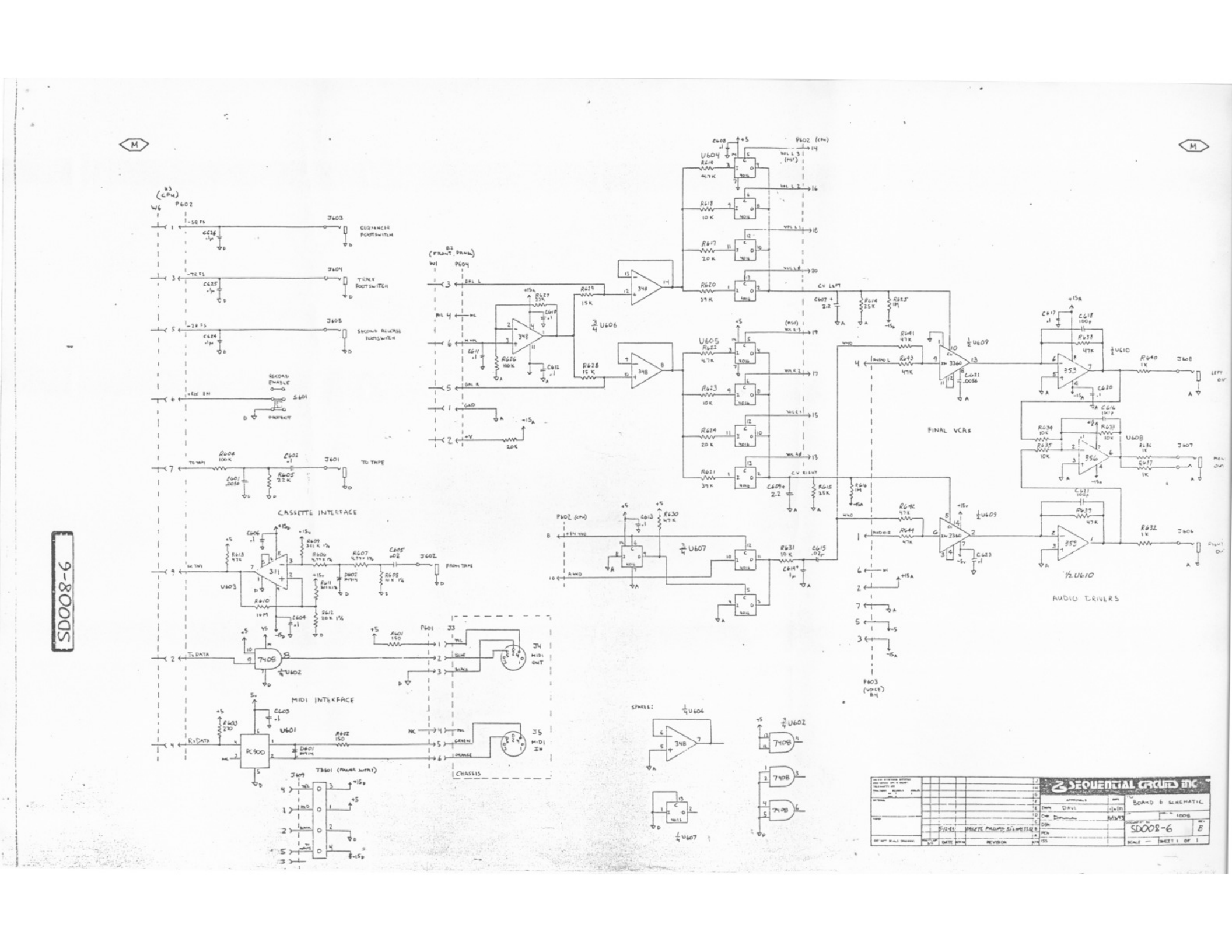
These are the only chips powered by -12V.

U365/66	Synth Switch Latches Similar to U359/60.	I-228	4174 HEX LATCH
U367	Misc Logic See U309-8.	I-248	74HC02

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
3.11.2	**OTHER PARTS**		
BT301	Non-Volatile Battery	E-040	2.9V LITHIUM BATTERY
C301		C-020	1.0 25V 20% TANT RADIAL
C302		C-045	.1 50V 20% MONO RADIAL
C303		C-023	47 10V 20% TANT RADIAL
C304-10		C-045	.1 50V 20% MONO RADIAL
C311		C-020	1.0 25V 20% TANT RADIAL
C312-23		C-045	.1 50V 20% MONO RADIAL
C324		C-002	10 pF 50V 10% DISC RADIAL
C325-32		C-045	.1 50V 20% MONO RADIAL
C340/41		C-045	.1 50V 20% MONO RADIAL
D301/02		D-008	1N34
D303/04		D-005	1N914
D305/06		D-008	1N34
	D306 is kludged on solder side of PCB 3.		
J301/02		J-007	16-PIN DIP SOCKET
J303-05	Used with P303-05	J-085	JUMPER JACKS
J306	Power Connector	J-047	9-PIN JACK
	For J306	P-028	GOLD JACK PINS
P301		P-043	20-PIN HEADER
P302		P-083	40-PIN LOCKING HEADER
P303-05		P-080	2-PIN SINGLE ROW HEADER
R301		R-076	27K
R302		R-044	270K
R303		R-025	100K
R304		R-008	1K
R305-07		R-012	10K
R308-12		R-025	100K
R313-15		R-010	2K
R316-18		R-012	10K
TP301	Disables memory access of Main system when tied high.		
TP302	Main -NMI		
TP303	Main -BREQ		
TP304	Final -NMI		
TP305	Final -BREQ		
TP306	Final -MO		
		J-016	40-PIN DIP SOCKET
		J-017	24-PIN DIP SOCKET
		J-045	28-PIN DIP SOCKET
		J-082	20-PIN DIP SOCKET
		PC1008-3	PCB 3

Rev B required a Main WRITE line jumper.
Rev C added diode memory protect.
Rev D has no mods.

SCHEMATIC
sheet M
SD008-6 1/1
50% reduction
11x17


SD008-6
P602 (CPU)
J603
SEQUENCER FOOTSWITCH
J604
TRACK FOOTSWITCH
J605
SECOND RECORD FOOTSWITCH
RECORD ENABLE
S601
PROTECT
J601
TO TAPE
CASSETTE INTERFACE
J602
FROM TAPE
U603
MIDI INTERFACE
U601
PC900
7408
J609
73601 (POWER SWITCH)
J3
J4
MIDI OUT
J5
MIDI IN
CHASSIS
P601
P604 (FRONT PANEL)
U604
U605
CV LEFT
CV RIGHT
FINAL VCA's
AUDIO DRIVERS
P603 (VOICE BD)
SPARES:
SEQUENTIAL CIRCUITS INC.
BOARD & SCHEMATIC
SD008-6
B
SHEET 1 OF 1

PCB 6 DESIGNATOR MAP
~~show solder side up--desig map may have to be reversed~~
PP008-6
1:1
11 x 17

6.1 AUDIO OUTPUT FUNCTIONAL TEST

For audio problems not covered in this section, see also section 4/5.

For other back panel functions, see

CASSETTE (TO/FROM TAPE)	O.17-19
SEQUENCER FOOTSWITCH	3.9
UNISON/TRACK FOOTSWITCH	K.5
2ND REL FOOTSWITCH	4/5.18, step 17
MIDI IN/OUT	3.11

1. Select basic test program (see page 4/5.9).

2. Switch A-440 on.

   You want to use A-440 (rather than the synthesizer) to test the audio output because it is basically independent of the synthesizer.

6.1.1 RIGHT FUNCTIONAL TEST

1. Check that PROGRAMMER RIGHT is on.

2. Turn BALANCE to RIGHT (5).

3. Turn the black PROG VOLUME knob to 10.

   The decimal point in the RIGHT PROGRAM display will light to indicate the current program has been edited.

4. Rotate PROG VOLUME from 10 down to 0.

   This knob is quantized to four bits (16 steps), so the effect will not be entirely smooth. But the attentuation should be continuous.

5. When PROG VOLUME is minimum, no A-440 should bleed-through (i.e., be audible). Turn up monitor system to confirm this. Then turn it back down!

   Note: Due to hardware insurance provided for the ADC, all of the -T8's programmable (black) knobs really only operate from about "2" to about "8" on their dials.

6. Return PROG VOLUME to 10.

6.1.2 LEFT FUNCTIONAL TEST

1. Switch PROGRAMMER LEFT on.

2. Turn BALANCE to LEFT (5).

3. Turn the black PROG VOLUME knob to 10.

   The decimal point in the LEFT PROGRAM display will light to indicate the program has been edited.

4. Rotate PROG VOLUME from 10 down to 0.

   The effect will not be entirely smooth. But the attentuation should be continuous.

5. When PROG VOLUME is minimum, no A-440 should bleed-through (i.e., be audible).

6. Return PROG VOLUME to 10.

6.1.3 BALANCE/MASTER VOLUME FUNTIONAL TEST

1. Rotate BALANCE from LEFT to RIGHT, checking for smooth and symmetrical control.

   It may not be possible to completely turn off both sides. Total attenuation may be 60 - 80 dB.

2. Check for smooth, quiet control throughout MASTER VOLUME range.

3. Check that when MASTER VOLUME is at 0, there is no output (bleed-through).

   To hear this, increase monitor system gain.
   (Turn volume back down!)

4. Connect stereo headphones to MONO AUDIO OUTPUT jack, and check the MASTER VOLUME range.

   Both sides of the headphones should be driven with the monophonic signal.

5. Adjust BALANCE.

   When BALANCE is centered, the A-440 tone will appear a little louder than when it is to one side.

6. Center BALANCE.

7. Unplug headphones from MONO.

8. Adjust MASTER VOLUME to comfortable level.

9. Switch A-440 off.

6.2 REMOVING PCB 6

1. Raise boards (see page O.21).

2. PCB 6 is located on the right, mounted to the back panel.

3. Remove the four connectors going to PCB 6, then disconnect the wiring assembly from PCB 6 to the power supply board. (When reconnecting the ribbon cable, it should point down towards the case.)

4. To remove the board, remove all of the phone jack mounting nuts.

5. Note that the three AUDIO OUTPUT jacks are grounded to the back panel. But the five other jacks are insulated from the back panel with a bakelite spacer (inside) and fiber washer (outside).

Figure 6.2.1
BACK PANEL JACK MOUNTING

6.3 DUAL FOOTSWITCH

The footswitch included with the -T8 is a durable, noiseless design. The only service it may ever need is to install longer cables needed to reach the -T8 if it is mounted high up in a keyboard stack.

If replacing cables, do so one at a time so there is a model for routing the cable through the mechanism. To prevent squeaking, the unit must be reassembled correctly.

If lubrication is ever needed, do not use oil or grease. It will collect dust and deteriorate the molded parts. Instead, use teflon powder sparingly.

If the pedal (tongue) bends down due to fatigue, the angle-adjustment screw can be turned when its locknut is loosened.

6.4 PCB 6 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-275	PCB 6 ASSEMBLED
6.4.1		**CHASSIS**	
		S-064	DUAL FOOTSWITCH
	MIDI Cable	Z-293	DIN CONN SUBASSY
J3		J-069	6-PIN HOUSING
		P-031	POLARIZING PIN
		P-049	SOCKET PINS
J4/5	MIDI IN/OUT	J-071	5-PIN DIN JACK

6.4.2 INTEGRATED CIRCUITS

U601 MIDI Optoisolator I-330 PC900

Buffers MIDI IN data, becoming RxData to the UART. It contains an input LED and output phototransistor. When the LED turns on, the phototransistor connects the output pin (4) to ground.

If there is no input, R603 pulls pin 4 high. High data input on J5-5 reverse-biases the LED so it does not turn on, and RxDATA remains high. Low data on U601-2 lights the LED, which is being forward-biased through J5-4. This turns on the transistor, which pulls RxDATA low to ground. D601 protects the optoisolator from transmitter variations. Note that J5 is not grounded. This prevents formation of a ground loop.

U602-8 MIDI Driver I-004 7408 QUAD AND

Buffers Transmitter data out (TxDATA) from the UART (on PCB 3) to MIDI. This gate can sink up to 16 mA. When data is low, R601 turns on the receiver's optoisolater. J4 grounds the cable shield to the chassis.

U603 Cassette Comparator I-301 311 PRECISION CPR

Converts ac-coupled data from tape into digital pulses which are read by the Main system's Miscellaneous Input Port. With no input, R613 pulls open collector output pin 7 high. Divider R611/12 fixes the noninverting input at +0.93V. The inverting input is biased at the same point, for R609 equals R611, and R606/07/08 equal R612. It therefore only takes a slight positive voltage from C605 on pin 3, to drive the comparator output negative. D602 limits the negative value of the input. R610 provides positive feedback to accelerate switching speed.

U604 Left Prog Volume DCA I-206 4016 QUAD ANALOG SWITCH

The Digitally-Controlled Attenuator is a DAC (Digital-to-Analog Converter) which uses what is normally the DAC reference point as an input. The input signal is the buffered LEFT VOLUME CV as adjusted by the BALANCE and MASTER VOLUME knobs. The DCA control bits come from U325 Programmable Volume Latch. If all bits are low, the switches are open and no CV passes. As PROGRAMMED VOLUME is increased, the switches close in typically binary sequence, gradually decreasing the total parallel resistance. This divides the LEFT CV by the ratio of the DCA resistance to R614. C607 filters the "staircase" produced by the active switches.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U605	Right Prog Vol DCA Similar to U604.	I-206	4016 QUAD ANALOG SWITCH
U606	Volume CV Summers	I-313	LM348 QUAD 741 OP AMP

MVOL comes from the wiper of the MASTER VOLUME knob, which is wired between ground and +15V as provided by R645 (see P604-2). The ratio of R627 to R626 makes the buffer into a 1/3 divider, reducing this 15-V signal to a 5-V range.

R629/28 form the tops of two dividers. The bottom parts of each divider is the resistance betwen one end of the BALANCE knob, and its wiper, which is grounded. So when turned to LEFT, BAL R will be grounded, shunting MVOL to ground on the right.

In early production versions (Rev B), pin 4 had to be jumpered to the +15V supply from U608.

U607	A-440 Switch	I-206	4016 QUAD ANALOG SWITCH

The A-440 signal can be added to both audio sides by a switch which is controlled from the Main system's Miscellaneous Output Port. When EN A-440 is low, pins 9 and 5 are pulled high by R630. Switch U607-3 is on, shorting the A-440 line (pin 11) to ground to prevent leakage. When EN A440 goes high, pin 9 goes low, which lifts the ground connection, and U607-11 connects the A-440 to filter R631/C614 (which rounds the otherwise square waves), and C615 which ac-couples A-440 to the Left and Right VCAs.

U608	Mono Out Driver	I-323	LF356 FET OP AMP

U608 sums together a MONO output which drives a stereo jack, for headphones.

U609	Left/Right Volume VCAs	I-327	3360 DUAL VCA

The Left and Right Final VCAs combine the AUDIO L and R signals from the synthesizer with A-440, and feed the output drivers. R625 and R616 negatively-bias the CV inputs to ensure complete volume cutoff when there is no CV from the DCA.

U610	Left/Right Output Driver	I-335	LF353 DUAL FET OP AMP

If the audio output goes dead when stereo plugs are used, check that if the board is Rev C or earlier, there is a piece of insulating foam positioned between the jack and the board. (This is required to insulate the signal from the ground plane which runs under these jacks. This ground plane was removed from Rev D boards and above.)

HARDWARE DESCRIPTION

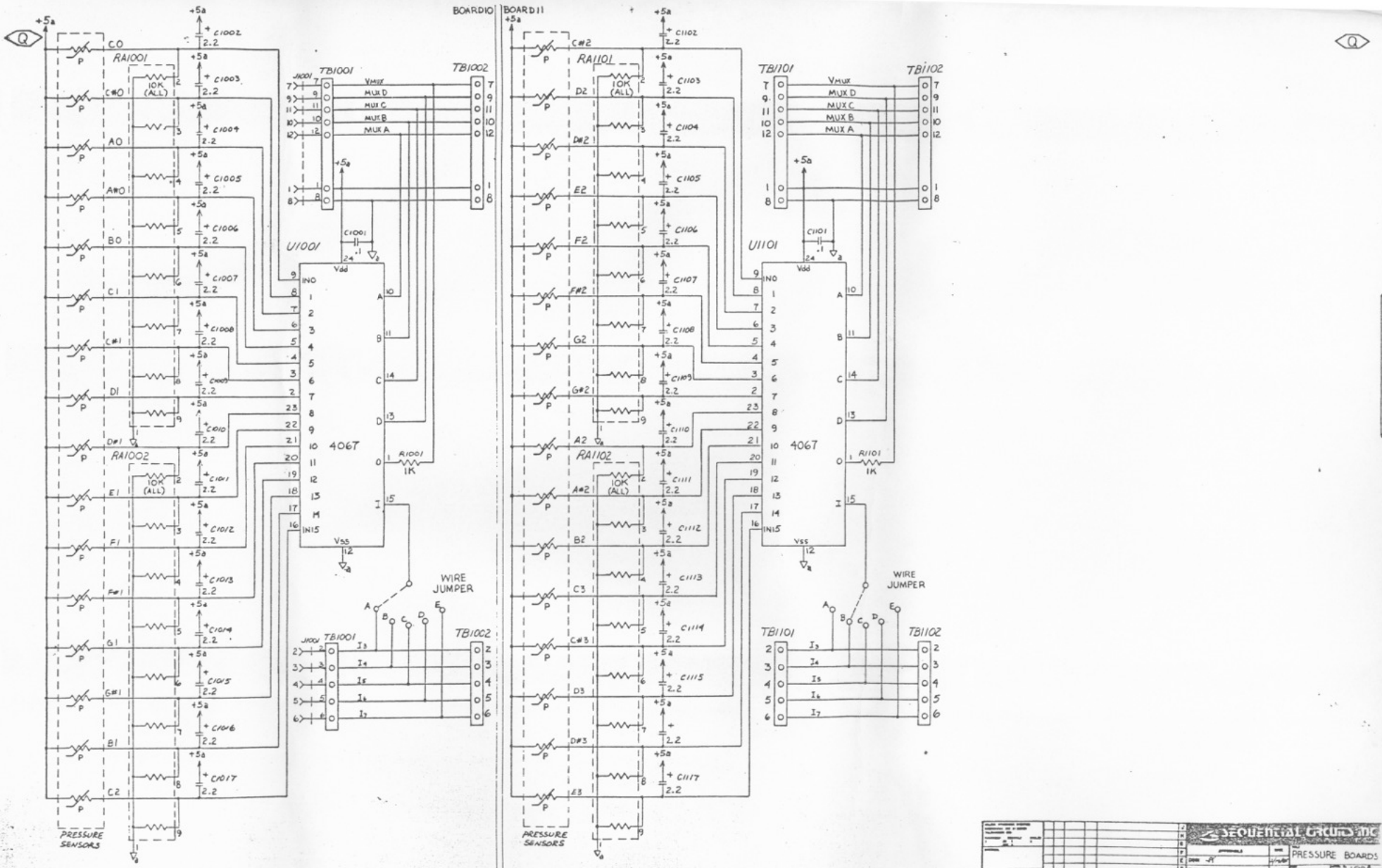
DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
C601		C-046	.0056 100V MYLAR RADIAL
C602-04		C-045	.1 50V 20% DISC RADIAL
C605		C-014	.02 50V 20% DISC RADIAL
C606		C-045	.1 50V 20% DISC RADIAL
C607		C-081	2.2 50V ELECT LOW LEAK
C608		C-045	.1 50V 20% DISC RADIAL
C609		C-081	2.2 50V ELECT LOW LEAK
C610-13		C-045	.1 50V 20% DISC RADIAL
C614		C-080	1 50V ELECT LOW LEAK
C615		C-014	.02 50V 20% DISC RADIAL
C616		C-004	100 pF 50V 10% DISC RADIAL
C617		C-045	.1 50V 20% DISC RADIAL
C618		C-004	100 pF 50V 10% DISC RADIAL
C619	not used		
C620		C-045	.1 50V 20% DISC RADIAL
C621		C-004	100 pF 50V 10% DISC RADIAL
C622-26		C-045	.1 50V 20% DISC RADIAL
D601/02		D-005	1N914
J601	TO TAPE	J-078	PHONE JACK MONO PC
J602	FROM TAPE	J-078	PHONE JACK MONO PC
J603	SEQUENCER FTSW	J-078	PHONE JACK MONO PC
J604	UNISON/TRACK FTSW	J-078	PHONE JACK MONO PC
J605	SECOND RELEASE	J-078	PHONE JACK MONO PC
	To insulate these	M-423	FIBER WASHER
	five jacks	M-424	BAKELITE WASHER
J606	RIGHT AUDIO	J-078	PHONE JACK MONO PC
J607	MONO AUDIO	J-079	PHONE JACK STEREO PC
J608	LEFT AUDIO	J-078	PHONE JACK MONO PC
	To ground these three AUDIO jacks.	M-182	3/8" STAR WASHER
	(Only required under audio jacks on pcb revs A-C)	M-117	SELF-ADHESIVE FOAM TAPE
J609/ TB601	PCB6 Power Connector	J-047	9-PIN JACK
	Needed for J-047	P-028	GOLD PIN
	Back Panel Power Cable	Z-287	PCB 6 WIRING SUBASSY
P601	MIDI IN/OUT	P-067	6-PIN LOCKING MOLEX
P602	I/O, PROG VOL	P-043	20-PIN HEADER
P603	Audio/Analog Pwr Input	P-078	7-PIN LOCKING MOLEX
	In Rev B, pin 1 (of P603) had to be trimmed away from the ground plane on top of board.		
P604	BALANCE/MVOL	P-067	6-PIN LOCKING MOLEX

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R601/02		R-402	150
R603		R-403	270
R604		R-025	100K
R605		R-040	22K
R606/07		R-107	4.99K, 1%
R608		R-108	10.0K, 1%
R609		R-115	301K, 1%
R610		R-045	10M
R611		R-115	301K, 1%
R612		R-144	20.0K, 1%
R613		R-011	4.7K
R614/15		R-037	7.5K
R616		R-029	1M
R617		R-015	20K
R618		R-012	10K
R619		R-011	4.7K
R620/21		R-017	39K
R622		R-011	4.7K
R623		R-012	10K
R624		R-015	20K
R625		R-029	1M
R626		R-025	100K
R627		R-054	33K
R628/29		R-014	15K
R630		R-018	47K
R631		R-012	10K
R632		R-008	1K
R633-35		R-012	10K
R636/37		R-008	1K
R638/39		R-018	47K
R640		R-008	1K
R641-44		R-018	47K
R645		R-015	20K
S601	RECORD PROTECT	S-063	SLIDE SW PC MOUNT
		J-027	14-PIN DIP SOCKET
		PC008-6D	BACK PANEL PCB

When set to "PROTECT", grounds U320-12 and U302-9 to prevent recording.

Rev B had a missing resistor, audio out pin shorted to ground, and problems at U606/08.
Rev C required removal of ground plane under audio jacks.
Rev D requres no mods.

SCHEMATIC Q
SD1008-10/11
50% reduction
11 x 17
Black Line

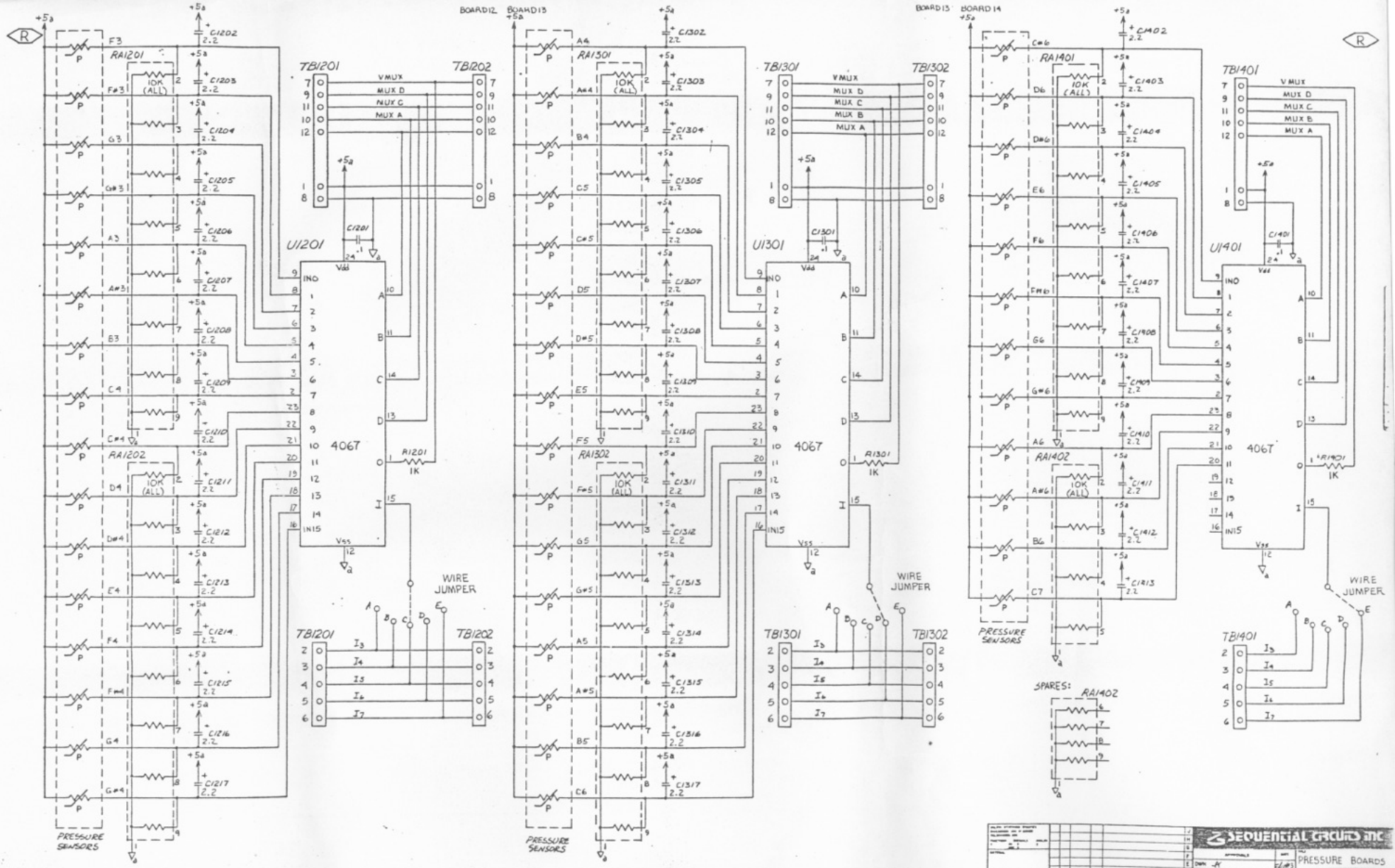


SEQUENTIAL CIRCUITS INC.

PRESSURE BOARDS

SD008-10/11

SCHEMATIC R
SD008-12/13/14
50% reduction
11 x 17
Black Line


BOARD12
BOARD13
BOARD13
BOARD14
RA1201
RA1202
RA1301
RA1302
RA1401
RA1402
10K (ALL)
TB1201
TB1202
TB1301
TB1302
TB1401
VMUX
MUX D
MUX C
MUX B
MUX A
U1201
U1301
U1401
4067
WIRE JUMPER
PRESSURE SENSORS
SPARES: RA1402
SEQUENTIAL CIRCUITS INC.
PRESSURE BOARDS
5D008-12/15/14
SCALE
SHEET 1 OF 1

PCB 10 DESIG MAP
PP008-10
50% reduction
11 x 17

~~Color~~ Black only

PRESSURE BOARD INSTALLATION DWG
DZ289
50% reduction
11 x 17
Black Line

10-14.1 PRESSURE SENSOR DIAGNOSTICS

The functional test of the Pressure system is given in the Keyboard section (see page K.4). These diagnostics are used to critically evaluate the pressure system.

The Pressure PCBs are part of the Main (Z-80) computer system. The pressure sensor diagnostics are contained in the special "DT8_4" EPROM which is required to test the Z-80 system (order SCI #Z-1017.)

1. Switch power off.

2. Remove the top panel (see page O.20).

3. From PCB 3 (at the left) remove U322, MAIN ROM. (Observe cautions discussed on page 3.14)

4. Orient DT8_4 EPROM correctly, with end notch facing left, and install.

5. If Z-80 was disabled for Z-8002 test, unground the Z-80 BREQ test point. (Ignore this step if you have not yet run Z-8002 diagnostics.)

6. Disable Z-8002 by clipping the Final BREQ test point (located just above U348) to ground. There is a GND test point in the middle of the board.

7. Switch power on. The control panel will not light. The Main system is waiting for a bank of diagnostics to be selected. There are two banks of tests in the DT8_4 EPROM:

	Page
Bank 1 = MAIN computer system diagnostics	
M1 I/O Test	3.16
M2 LED Test	1/2.11
M3 Local RAM Test	3.17
M4 Common RAM Test	3.17
M5 ADC Test (pots, pressure sensors, wheels)	1/2.11, 10-14.7
Bank 2 = KEYBOARD tests for calibration and debugging	
K1 Optics (unmounted), looped scan test	7-9.11
K2 Optics (mounted), single step scan test	7-9.10
K3 Pressure sensor (looped scan) test	10-14.8
K4 Pressure sensor (single step scan) test	10-14.9
K5 Optics (mounted), looped scan test	7-9.9
K6 Pressure sensor slope analyzer test	10-14.10

8. Main is selected at first. After this, to select a MAIN test, you must first press the LEFT program switch, selecting Test Bank 1. The The LEFT and RIGHT displays will read "(blank) 1" and "1 1" respectively for four seconds. The displays will then go blank. Pressing PROG/SEQ switches 1-5 will then select MAIN tests M1-M5.

9. To select one of the KEYBOARD tests, you must first press the RIGHT program switch, selecting Test Bank 2. The left and right displays will read "(blank) 2" and "2 2" respectively. The displays will then go blank. Pressing PROG/SEQ switches 1-6 will select KEYBOARD tests K1-K6.

10. The following tests are related to the pressure system: M5, K3, K4, and K6. (Instructions for each test follow in this section.)

11. When done testing the pressure sensors, you can perform the Main computer or optical system diagnostic tests (listed above), or perform the Final computer diagnostics (see page 3.19), or return to normal operation.

12. When all diagnostics are concluded, to resume normal operation:

a. Switch power off and install the operating PROM.

b. Remove BREQ ground from Z-8002.

c. Switch power on. (If the Main Common Ram test was run, no programs will be heard because they have been erased. A-440 won't be heard because PROG VOLUME has been set to 0 in the Scratchpad.

d. Reinitialize the PITCH wheel (see page 1/2.6).

e. Reload programs (and sequences) through the cassette interface.

f. Because the test clears the Scratchpad, you must select both a program on the LEFT side and one on the RIGHT side. (This fills the Scratchpad from the Program memory.)

10-14.1.1 M5 ADC DIAGNOSTIC TEST

Setup conditions for this test are described on page 10-14.5.

This test reads all pots (except MASTER VOLUME and BALANCE), the PITCH and MOD wheels, and all pressure sensors for proper ADC action. The converted hexadecimal value 00H to FFH is shown in the Right PROGRAM display.

1. If you have selected Bank 2 of the diagnostic tests, press LEFT. The display will read "(blank) 1" and "1 1" for four seconds before going blank.

2. Wait for the displays to clear.

3. Press 5. A decimal number should appear in the RIGHT display.

Note: Set both wheels fully down.

Note: Rotate all pots fully counterclockwise, to -5 or 0 (ignore BALANCE and MASTER VOLUME).

The display will read 00.

Selectively apply pressure to keys of interest to check digitization. Press only one key at a time. The display will increment. All keys must read from 00 through E0.

This diagnostic can be used in conjunction with the pressure threshold adjustment, to precisely indicate when the threshold has been crossed (values 00-01H). However, for threshold adjustment it will probably be more convenient to use test K3 (see next page).

This test has checked basic multiplexer and ADC operation. For a finer reading of sensor quality, test K6 is used. (See below.)

10-14.1.2 K3 PRESSURE SENSOR (LOOPED SCAN) DIAGNOSTIC TEST

Setup conditions for this test are described on page 10-14.5.

See pressure threshold adjustment procedure on page K.8. The only way to trim the keyboard is by trial and error, as you learn how much adjustment makes how much difference.

Using this test, when the threshold is reached, the LEFT and RIGHT LEDs will go on. At the same time, a tone will be heard from the AUDIO OUTPUT, and a scope connected to the TO TAPE jack will see a change of state.

1. If you have not yet selected Bank 2 of the diagnostic tests, press RIGHT. The LEFT and RIGHT displays will read "(blank) 2" and "2 2" respectively for four seconds before going blank.

2. Wait for the displays to clear.

3. Press 3. It will blink rapidly. The LEFT display should read 00. With no keys held, if the LEFT and RIGHT LEDs are on, this may indicate a shorted sensor. Use next test (K4) to isolate the problem.

4. Using the pressure gauge, press any key with a specified force of 550 (+/- 150 grams. (Depending on the sensitivity of the player, 400 - 700 grams may be preferred.)

   a. If the LEDs and tone indicate threshold before 400 grams is reached, increase threshold by tightening the actuator.

   b. If more than 700 grams doesn't produce an indication, decrease threshold by loosening the actuator.

   c. If no amount of pressure produces an indication, remove the key and press directly on the sensor foam. If there is still no reading, there is a problem either with the sensor, its filter capacitor, or multiplexer chip (U1001-1401)

5. Increasing pressure on the key beyond the threshold point will cause the LEFT display to count up to 7. If this count skips any numbers, the sensor should probably be replaced.

6. When the sensor is released, the display should count down quickly. If it doesn't, this may indicate that the pull-down resistor (in the resistor array) for that sensor is open.

10-14.1.3 K4 PRESSURE SENSOR (SINGLE STEP SCAN) DIAGNOSTIC TEST

For test setup instructions, see page 10-14.5.

This test is similar to K3, but allows you to program the multiplexer to read any single key. This may be useful for isolating malfunctions (because all of the multiplexer outputs are tied together).

1. If you have not yet selected bank 2 of the diagnostic tests, do so now by pressing RIGHT. The LEFT and RIGHT displays will read "(blank) 2" and "2 2" respectively for four seconds before going blank.

2. Wait for the displays to clear.

3. Press 4. The RIGHT will display 01, which is the number of the first key (key numbers are stamped on the wood). When only the indicated key is pressed, pressing will produce the same indications as in test K3, above.

5. To advance to the next key, press PROGRAM/SEQUENCE 8.

10-14.1.4 K6 PRESSURE LINEARITY DIAGNOSTIC TEST

Setup conditions for this test are described on page 10-14,5.

The linearity of a pressure sensor is its ability to respond to the force exerted in continuous, analog fashion. This linearity is most important when the pressure signal is used to bend oscillator pitch, as any bumps in the response curve will appear as erratic pitch. Therefore we estimate sensor quality in terms of semitones. A sensor should have no gaps exceeding 3 semitones anywhere in its range.

As you press a key, this test looks at the ADC values which are generated. When the measurement crosses value D0H, measurement stops. The computer then stops conversion and displays a decimal number which classifies sensor quality according to the following table:

Display	Sensor Quality
00	sensor reaches max value but data insufficient. (Usually means you pressed the sensor too quickly.)
11	full pass. No jumps exceeding 3 semitones (related to frequency-bending)
4	4-semitone jump
47	4- to 7-semitone jump
7	7-semitone jump
79	7- to 9-semitone jump
88	sensor is acting almost like a switch

This test requires you to develop a feel for how fast to press the key. Press smoothly --neither too slowly nor too quickly--to see each increment (you are in effect entering each number which appears into a calculation).

1. If you have not yet selected Bank 2 of the diagnostic tests, do so now by pressing RIGHT. The LEFT and RIGHT displays will read "(blank) 2" and "2 2" respectively for four seconds before going blank.

2. Wait for the displays to clear.

3. Press PROGRAM/SEQUENCE 6. The RIGHT display will read 01, which is the number of the first key (key numbers are stamped on the wood). The LEFT display shows the HEX ADC value of the active sensor. This is initally 00.

4. Press the key with increasing force, until the display reads E0. (You will not actually see E0 because it is only on briefly.) If you allow the key to slip back, it is best to restart the test (by pressing PROGRAM/SEQUENCE 7.)

> If the display does not read "11", retest the key to make sure you did not accidentally slip back when applying pressure.

5. The sensor quality code number will appear in the LEFT.

6. Repeat the test as required to verify results. To clear the test result and retest the same sensor, press PROGRAM/SEQUENCE 7. To advance to the next key, press 8.

10-14.2 ACCESS TO PRESSURE BOARDS

The five pressure sensor boards are located under the keys. (See drawing, page 10-14.4.) Each board can be electrically probed after the keys above it are removed.

1. Remove the control panel (see page 1/2.12).

2. Each key has a number stamped on it, from 1 to 76. Keys are assigned to boards as indicated:

Board #	Keys
10	1-16
11	17-32
12	33-48
13	49-64
14	65-76

3. To remove a key, raise the hammer then lift the key off of its pivot pin.

4. When replacing a key, again lift the hammer so that the felt "pedestal" area is not damaged by being forced against the capstan.

10-14.3 PRESSURE SENSOR REPLACEMENT

At this point you have performed the functional test, checked the pressure threshold (see KEYBOARD section), and used the diagnostics to troubleshoot and repair the electronics. Now the work comes to replacing defective sensors themselves.

> Note: The schematics show the serial number ranges of early machines which used different values of pull-down resistors--to match the characteristics of early-production sensors. Therefore if a sensor is replaced on one of these early machines, it may be necessary to change the value of its pull-down resistor as well, to provide a satisfactory response. (Unfortunately it may be necessary to remove the board to do this, because the work will involve removing the SIP network and replacing it with discrete resistors.)

Sensor replacement is explained below. Start with the worst sensor first. After you see what is involved to replace it, you can then decide which of the remaining questionable sensors you can live with or not. The sensor itself comes on a strip of sixteen, for mounting one complete board. To repair a sensor you basically have to cut through the existing foam and sensor strip, completely remove the sensor and clean the area, then install the new sensor (SCI #MS008-1A, 16 sensors) and foam (SCI #MS008-2A, covers 16 sensors).

> Note: When replacing pressure sensors, the sensor bottom and gold pads must be absolutely clean. Any contamination between the sensor and pads will cause non-linearities.

> Note: Due to the small amount of adhesive used to secure the sensors, it is usually necessary to replace at least **two** adjacent sensors at a time even though only one of the sensors needs replacing. The following procedure assumes that at least two sensors will be replaced at a time. The question of which of the adjacent sensors should be replaced is not critical, so replace whichever of the two is worse.

To replace sensors:

1. Remove several keys from around the affected sensors.

2. Slice through the foam and strip on either side of the sensors to be replaced.

3. Pull off foam and sensors from board.

4. Clean old adhesive from board with solvent (Freon) and cotton swabs. Don't get any solvent near the adjacent sensors.

5. Allow solvent to dry completely.

6. Make sure there are no conductive particles (like gold flakes), fingerprints, nor any foreign material on or between pads.

7. Cut replacement sensors from strip. (Your caution and cleanliness during what follows will be rewarded. So will carelessness!)

8. Remove all paper backing from sensors.

9. Inspect the sensors. The conductive, black side must be completely smooth and clean. Any lumps, dirt or oil may cause erratic sensing. On the back side, there should be no scratches on the black dots that allow any of the silver to show through. Any sensor that shows silver through to the backside must be rejected as it will cause the sensor to be shorted. (Smear lines on the black dots are probably acceptable.) If the sensor is at all questionable according to these criteria, do not use it. Cut another one from the strip.

10. Position the sensors squarely over the pads and apply it.

11. Add new foam. (Don't even try to use the old foam.)

12. If diagnostics are available, test the new sensors.

13. Don't forget to check pressure threshold adjustment of all replaced sensors.

10-14.4 PRESSURE BOARD REMOVAL

This procedure is last because to either work on the sensors or replace the multiplexers the boards don't have to be removed.

If a multiplexer needs to be replaced on either PCB 10 (the lowest pressure board) or 14 (the highest one), remove the keys, unscrew the board, and tilt it up.

If a multiplexer needs to be replaced on the middle three boards, PCBs 11-13, rather than remove all of the boards to turn one of these over, instead remove the keyboard. All the 4067s will then be accessible from the underside of the keyboard frame.

If pressure boards must be unmounted, do not stress the interconnecting jumpers.

10-14.5 PCBS 10-14 HARDWARE DESCRIPTION

All five pressure boards are built from identical PC boards which buss the supply voltage, multiplexer addresses and enable strobes to each board.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-279A	PCB 10 ASSEMBLED
U1001	16-Channel Multiplexer	I-245	MC14067BCP (4067)

The 4067 connects 1 of its 16 analog inputs, to its output at a time. The input is selected by a binary number on the ABCD address inputs. For example, when ABCD is 0000, IN0 is selected and when ABCD is 1111, IN15 is selected. In addition to selecting the multiplexer channel, the computer selects one of the five pressure multiplexer ICs at a time, by using the Inhibit (I) input. When I is high, the output (pin 1) is inhibited (high-impedance). A wire jumper to one of the strobe lines I3-I7 defines the position of the board. When I goes low, the voltage of the selected sensor becomes Vmux, which is read by the ADC.

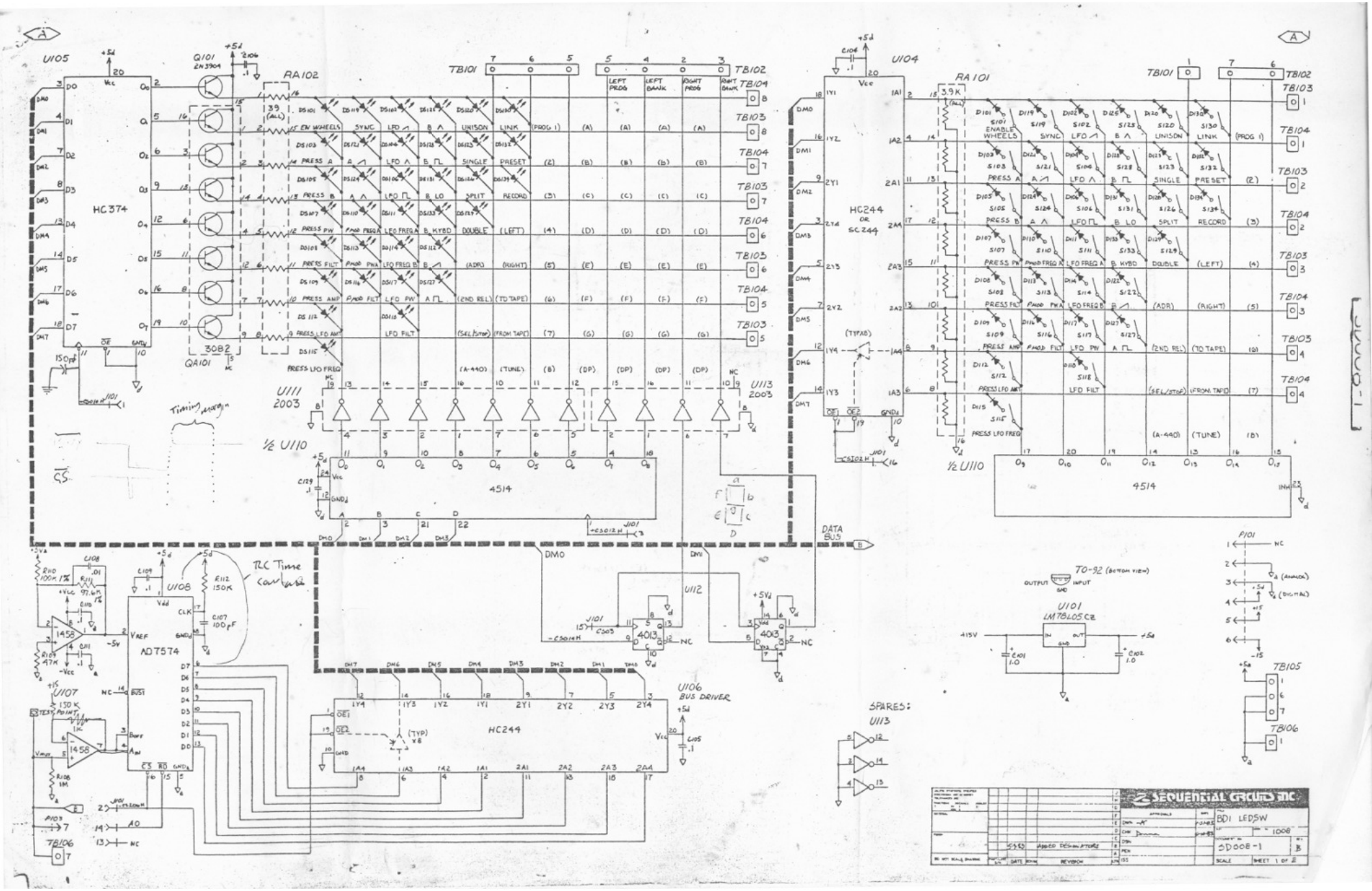
Note that when no keys are held, the pressure mux is not scanned.

Each sensor is wired in a divider circuit between the positive supply and a pull-down resistor. With no pressure applied, the sensor resistance is virtually infinite. Therefore the voltage at the divider point is virtually zero. With maximum pressure, resistance approaches a minimum of 10K. The voltage at the divider junction therefore increases towards the supply voltage as pressure is applied, providing an analog of the applied pressure. The capacitors filter smooth quick voltage fluctuations due either to sensor nonlinearity or playing technique.

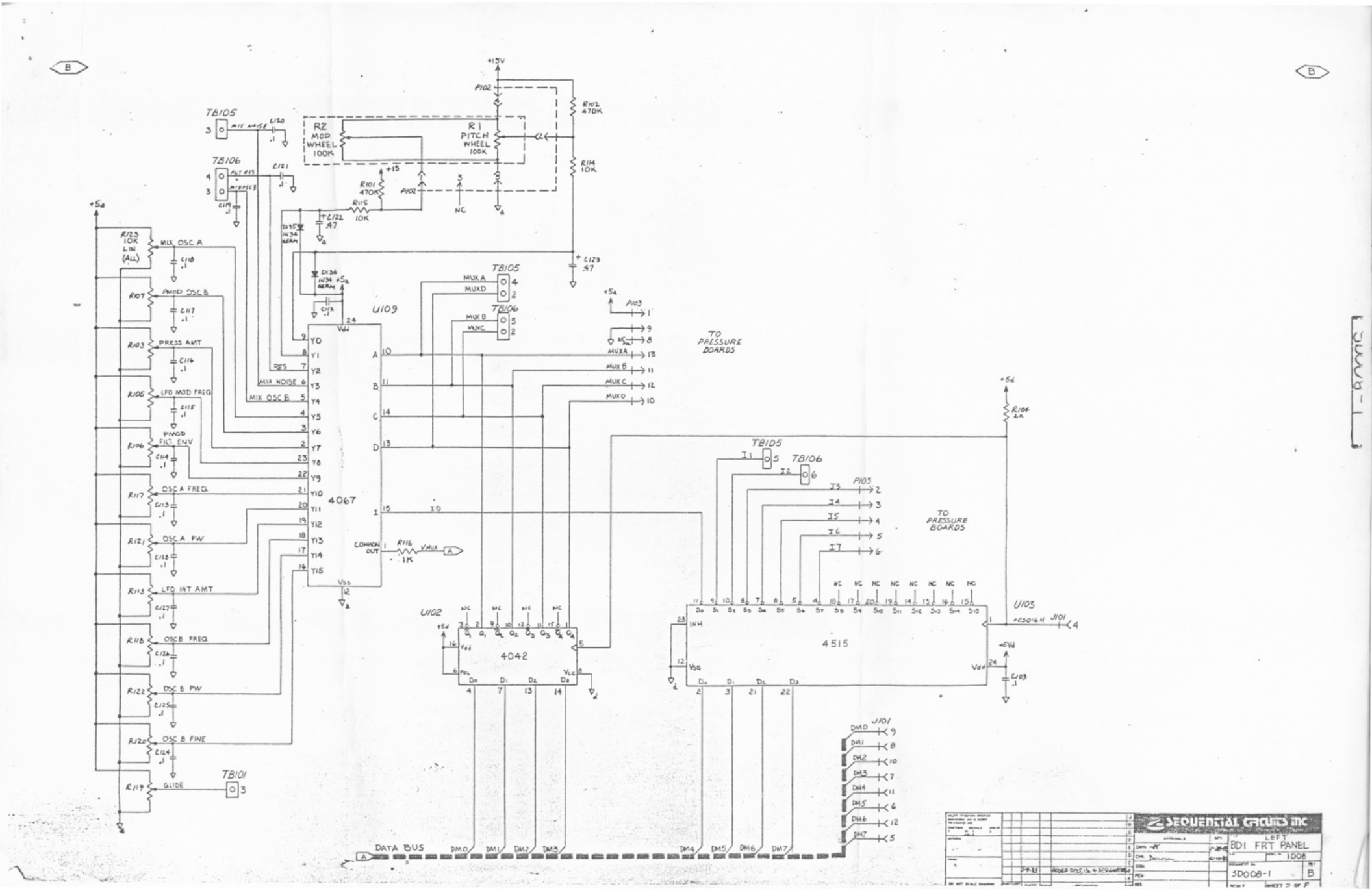
C1001		C-045	.1 50V MONO RADIAL
C1002-17		C-052	2.2 15V ELECT AXIAL
J1001	Pressure Mux Cable	E-143	12" 13-PIN HDR/BRAID
R1001		R-008	1K
RA1001/02		R-309	22K x 10 SIP ARRAY
		Z-279B	PCB 11 ASSEMBLED
U1101	16-Channel Multiplexer	I-245	MC14067BCP (4067)
C1101		C-045	.1 50V DECOUPLER
C1102-17		C-052	2.2 15V ELECT AXIAL
R1101		R-008	1K
RA1101/02		R-309	22K x 10 SIP ARRAY
TB1101		E-111	1" 12-WIRE JUMPER

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-279C	PCB 12 ASSEMBLED
U1201	16-Channel Multiplexer	I-245	MC14067BCP (4067)
C1201		C-045	.1 50V DECOUPLER
C1202-17		C-052	2.2 15V ELECT AXIAL
R1201		R-008	1K
RA1201/02		R-309	22K x 10 SIP ARRAY
TB1201		E-111	1" 12-WIRE JUMPER
		Z-279D	PCB 13 ASSEMBLED
U1301	16-Channel Multiplexer	I-245	MC14067BCP (4067)
C1301		C-045	.1 50V DECOUPLER
C1302-17		C-052	2.2 15V ELECT AXIAL
R1301		R-008	1K
RA1301/02		R-309	22K x 10 SIP ARRAY
TB1301		E-111	1" 12-WIRE JUMPER
		Z-279E	PCB 14 ASSEMBLED
U1401	12-Channel Multiplexer	I-245	MC14067BCP (4067)
C1401		C-045	.1 50V DECOUPLER
C1402-13		C-052	2.2 15V ELECT AXIAL
R1401		R-008	1K
RA1401/02		R-309	22K x 10 SIP ARRAY
	In Rev A (dark green) pin 1 of RA1401/2 must be tied together (otherwise the top four keys won't have pressure action).		
TB1401		E-1111"	12-WIRE JUMPER
Each board uses:		MS1008-1	16 PRESS SENS STRIP
	Covers 16 sensors	MS1008-2	PRESSURE STRIP FOAM
		PC1008-10	PRESSURE BOARD
Hold pressure boards to keyboard		M-208	#6 x 3/8" PH PHIL SMS

SCHEMATIC A
SD008-1 1/2 (BD1 LED, SW)
50% reduction
11 X 17
Black Line


U105
HC374
Q101
2N3904
RA102
TB101
TB102
TB103
TB104
LEFT PROG
LEFT BANK
RIGHT PROG
RIGHT BANK
EN WHEELS
SYNC
LFO
UNISON
LINK
PROG 1
PRESS A
LFO
SINGLE
PRESET
PRESS B
LFO
SPLIT
RECORD
PRESS PW
PMOD FREQ A
LFO FREQ A
B KYBD
DOUBLE
PRESS FILT
PMOD
LFO FREQ B
ADR
PRESS AMP
PMOD FILT
LFO PW
END REL
TO TAPE
PRESS LFO AMT
LFO FILT
SEL/STOP
FROM TAPE
PRESS LFO FREQ
A-440
TUNE
U111
2003
U113
2003
½ U110
4514
U104
HC244
OR
SC244
RA101
3.9K
ENABLE WHEELS
PROG 1
LINK
SPLIT
RECORD
LEFT
ADR
RIGHT
END REL
TO TAPE
FROM TAPE
SEL/STOP
PRESS LFO FREQ
A-440
TUNE
½ U110
4514
DATA BUS
U112
4013
4013
U108
AD7574
RC Time Constant
U107
1458
1458
U106
BUS DRIVER
HC244
SPARES:
U113
TO-92 (BOTTOM VIEW)
OUTPUT
INPUT
GND
U101
LM78L05CR
P101
TB105
TB106
SEQUENTIAL CIRCUITS INC.
BD1 LEDSW
5D008-1
SHEET 1 OF 2

SCHEMATIC B
SD008-1 2/2 (BD1 Left front panel)
50% reduction
11 X 17
Black Line


+15V
P102
R102 470K
R2 MOD WHEEL 100K
R1 PITCH WHEEL 100K
R114 10K
R101 470K
R115 10K
C122 .47
C123 .47
TB105
TB106
MIX NOISE SE
MIX OSC B
C130
C131
C119
D135 1N34 GERM
D136 1N34 GERM
+5d
R123 10K LIN (ALL)
MIX OSC A
C118
R107
PMOD OSC B
C117
R103
PRESS AMT
C116
R105
LFO MOD FREQ
C115
PMOD FILT ENV
R106
C114
R117
OSC A FREQ
C113
R121
OSC A PW
C128
R113
LFO INT AMT
C127
R118
OSCB FREQ
C126
R122
OSC B PW
C125
R120
OSC B FINE
C124
R119
GLIDE
TB101
U109
4067
RES
MIX NOISE
MIX OSC B
COMMON OUT
R116 1K
VMUX
MUX A
MUX D
MUX B
MUX C
P103
TO PRESSURE BOARDS
R104 2K
U102
4042
U103
4515
+5016H
J101
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DATA BUS
SEQUENTIAL CIRCUITS INC.
LEFT
BD1 FRT PANEL
1008
SD008-1
B
SHEET 2 OF 8

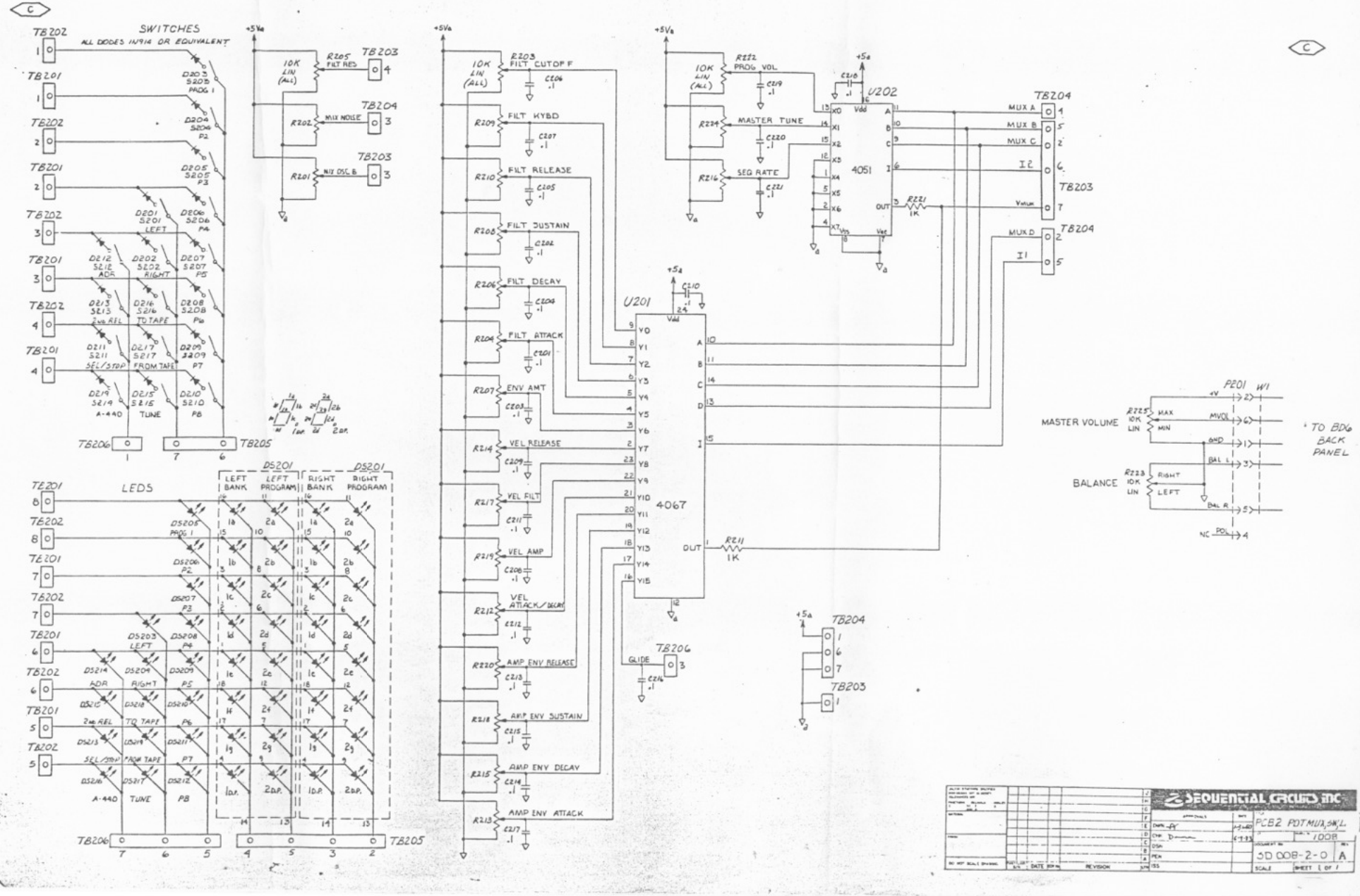
PCB 1 DESIG MAP
PP008-1 1/1
1:1
11 X 25

black screen: solder side
blue screen: comp side

PCB 2 DESIG MAP
PP008-2 1/1
1:1
11 X 25

black screen: solder side
blue screen: comp side

SCHEMATIC C
SD008-2 1/1 (POT MUX, SW, LED)
50% reduction
11 X 17
Black Line


SWITCHES
ALL DIODES IN4914 OR EQUIVALENT
LEDS
TB202
TB201
TB205
TB206
TB203
TB204
+5Va
10K LIN (ALL)
R205 FILT RES
R202 MIX NOISE
R201 MIX OSC B
R203 FILT CUTOFF
R209 FILT KYBD
R210 FILT RELEASE
R208 FILT SUSTAIN
R206 FILT DECAY
R204 FILT ATTACK
R207 ENV AMT
R214 VEL RELEASE
R217 VEL FILT
R219 VEL AMP
R212 VEL ATTACK/DECAY
R220 AMP ENV RELEASE
R218 AMP ENV SUSTAIN
R215 AMP ENV DECAY
R213 AMP ENV ATTACK
R222 PROG VOL
R224 MASTER TUNE
R216 SEQ RATE
R221 1K
R211 1K
U201
4067
U202
4051
MUX A
MUX B
MUX C
MUX D
I2
I1
VMUX
GLIDE
MASTER VOLUME
BALANCE
MAX
MIN
RIGHT
LEFT
MVOL
BAL L
BAL R
GND
NC
POT
P201
W1
+V
* TO BD6 BACK PANEL
DS201
LEFT BANK
LEFT PROGRAM
RIGHT BANK
RIGHT PROGRAM
PROG 1
P2
P3
P4
P5
P6
P7
P8
LEFT
RIGHT
ADR
2nd REL
TO TAPE
FROM TAPE
SEL/STOP
A-440
TUNE
1 DP.
2 DP.
SEQUENTIAL CIRCUITS INC.
PCB2 POTMUX,SW'L
1008
SD 008-2-0
A
SCALE
SHEET 1 OF 1

1/2.1 PITCH WHEEL INITIALIZATION PROCEDURE

Note: The PITCH wheel must be reinitialized after any diagnostic tests have been run, or after any computer repair which may affect non-volatile RAM, or after adjusting the wheel itself.

To initialize the PITCH wheel, the Main operating software must be installed and the instrument must be functioning normally.

1. Center the PITCH wheel solidly in its detent.

2. While holding the RECORD switch, press PROGRAM/SEQUENCE 3. This writes the current wheel position into memory for reference in detecting changes in wheel position.

3. Raise or lower the PITCH wheel, then return it to its center detent. This updates all operating parameters with the new reference value.

1/2.2 CONTROL PANEL FUNCTIONAL TESTS

The control panel consists of knobs, switches and LEDs. If any of these fails to work or fails to indicate, perform the functional test for that control module, to learn whether the fault is in the control panel (less likely) or in the circuitry controlled (more likely).

Bad switches are identified either by checking instrument function or the appropriate output latch, if the switch has a specific latch bit assigned to it (such as SYNC, Sawtooth, Triangle, the three POLY-MOD destination switches, or A-440. See pages 3.2 and 3.3).

If the DT8_4 EPROM is available, bad LEDs can be identified with the M2 diagnostic (see page 1/2.11). A bad knob or ADC can be idenitifed by using the M5 diagnostic (see page 1/2.11).

1/2.3 WHEEL FUNCTIONAL TESTS

1/2.3.1 PITCH WHEEL FUNCTIONAL TEST

1. Switch ENABLE WHEELS OFF.

2. Set the PITCH wheel to its lowest position.

3. Select the basic program (see page 4/5.9).

4. Switch A-440 on.

5. Play A4 (under PROGRAM/SEQUENCE 4 switch).

6. Adjust MASTER TUNE to eliminate "beating" between A4 and A-440.

7. Switch ENABLE WHEELS on.

   There should be a pitch change of about a minor third.

8. Check that the PITCH wheel bends notes up and down by at least a minor 3rd from its center position.

   There should be no pitch jitter as the wheel is turned slowly.

9. Return PITCH wheel to center.

   There should be no "beating" against A-440.

10. If A4 does not produce A-440 initialize the PITCH wheel (see page 1/2.6).

1/2.3.2 MOD WHEEL FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. In the LFO-MOD section:
   a. Turn FREQUENCY to 5.
   b. Switch triangle waveshape on.
   c. Switch FREQ A DESTINATION on.

3. Switch ENABLE WHEELS on.

4. While playing, check that the MOD wheel smoothly applies modulation.

5. Check that MOD wheel has the same maximum depth as INIT AMT.

6. Switch ENABLE WHEELS off.

7. While playing, move the MOD wheel to confirm that it is disabled.

8. Return MOD to minimum.

1/2.4 CONTROL PANEL DIAGNOSTICS

The Control Panel PCBs and Wheels are part of the Main (Z-80) computer system. The Potentiometer (pot) and LED diagnostics are contained in the special DT8_4 EPROM which is required to test the Z-80 system (order SCI #Z-1017.)

If the PROGRAM/SEQUENCE switches are malfunctioning, it may not be possible to select any diagnostic tests.

1. Switch power off.

2. Remove the top panel (see page O.20).

3. From PCB 3 (at the left) remove U322, MAIN ROM. (Observe cautions discussed on page 3.13)

4. Orient DT8_4 EPROM correctly, with end notch facing left, and install.

5. If Z-80 was disabled for Z-8002 test, unground the Z-80 BREQ test point. (Ignore this step if you have not yet run Z-8002 diagnostics.)

6. Disable Z-8002 by clipping the Final BREQ test point (located just above U348) to ground. There is a GND test point in the middle of the board.

7. Switch power on. The control panel does not light. The Main system is waiting for a bank of diagnostics to be selected. There are two banks of tests in the DT8-4 EPROM:

	Page
Bank 1 = MAIN computer system diagnostics	
M1 I/O port test	3.16
M2 LED test	1/2.11
M3 Local RAM test	3.17
M4 Common RAM test	3.17
M5 ADC test (pots, pressure sensors, wheels)	1/2.11, 10-14.7
Bank 2 = KEYBOARD tests for calibration and debugging	
K1 Test of unmounted optical system	7-9.11
K2 Single step test of key optics	7-9.10
K3 Looped scan of pressure sensors	10-14.8
K4 Single step test of pressure sensors	10-14.9
K5 Looped scan of optical system	7-9.9
K6 Pressure sensor slope analyzer test	10-14.10

8. Main is selected at first. After this, to select a MAIN test, you must first press the LEFT program switch, selecting Test Bank 1. The LEFT and RIGHT displays read "(blank) 1" and "1 1" respectively for four seconds, then go blank. Pressing PROG/SEQ switches 1-5 then select MAIN tests M1-M5.

9. To select one of the KEYBOARD tests, you must first press the RIGHT program switch, selecting Test Bank 2. The LEFT and RIGHT displays read "(blank) 2" and "2 2" respectively, then go blank. Pressing PROG/SEQ switches 1-6 select KEYBOARD tests K1-K6.

10. The test numbers for Pot and LED diagnostiocs are M2, M5, K3, K4, and K6. (Instructions for each test follow in this section.)

11. When done testing the control panel, you can perform the Main I/O, Local RAM, Common RAM or pressure sensor tests (listed above), or perform Final Computer diagnostics (see page 3.18), or return to normal operation.

12. When all diagnostics are concluded, to restore normal operation:

a. Switch power off and install the operating PROM.

b. Remove BREQ ground from Z-8002.

c. Switch power on. (If the Main Common RAM test was run, no programs will be heard because they have been erased. A-440 won't be heard because PROG VOLUME has been set to 0 in the Scratchpad.)

d. Reinitialize the PITCH wheel (see page 1/2.6).

e. Reload programs (and sequences) through the cassette interface.

f. Because the test clears the Scratchpad, you must select both a program on the LEFT side and one on the RIGHT side. (This fills the Scratchpad from the Program memory.)

1/2.4.1 M2 LED DIAGNOSTIC TEST

Setup conditions for this test are described on page 1/2.9.

1. If you have performed any of the Bank 2 diagnostic tests, you must first select Bank 1 by pressing LEFT and wait for the displays to clear after reading "(blank) 1" and "1 1" for four seconds.

2. Press 2.

All LEDs light in sequence. Replace the switch (the LED is integral) when individual LEDs don't light. If several LEDs fail to light, inspect the schematic (pages 1/2.1 and 1/2.5) for common components in a row or column of the matrix.

1/2.4.2 M5 KNOB ADC DIAGNOSTIC TEST

Setup conditions for this test are described on page 1/2.9.

This test reads all pots (except MASTER VOLUME and BALANCE), the PITCH and MOD wheels, and all pressure sensors for proper ADC action. The converted hexadecimal value 00H to FFH is shown in the Right PROGRAM display.

1. If you have performed any of the Bank 2 diagnostic tests, you must first select Bank 1 by pressing LEFT and wait for the displays to clear after reading "(blank) 1" and "1 1" for four seconds.

2. Press 5. A decimal number should appear in the RIGHT display.

Note: Set both wheels fully down.

Note: Rotate all pots fully counterclockwise, to -5 or 0 (ignore BALANCE and MASTER VOLUME).

The display will now read 00.

Selectively rotate one knob of interest at a time through its range to check digitization. All knobs, and the MOD wheel must reach FFH. With patience, it is possible to turn each control slowly enough to display each incremental value. (Don't mistake a "b" for a "6"--the top segment is not lit on the "b.") If a pot misses any numbers, it should be replaced. (If the warranty has elapsed, the owner should be allowed to decide whether the problem is actually noticable enough to justify the work involved to remove and replace one of the control PCBs.)

While this test is selected, pressure sensors can also be tested. (See page 10-14.7.)

1/2.5 UNMOUNTING THE CONTROL PANEL

This procedure is required to access PCBs 1 or 2, remove the side panels, or remove any keys or the entire keyboard.

1. Remove top panel (see page O.20).

2. Raise boards (see page O.21).
   (Note: this is only necessary if you are removing the control panel completely.)

3. Remove five screws along upper edge of control panel.

4. Remove two screws at each side of control panel.

Note: The screws on the left side (above the wheel box) have been cut very short to prevent damage to the edge of PCB 1. When installing the control panel, be sure that short screws are installed at these two places. In later production, 1/8" screws, SCI #M-473 were used in all four places.

If the control panel is unscrewed but not disconnected, it can be lifted up to allow keys to be removed. But if you lay the control panel on top, protect the top wooden edge from the sharp pins from the control panel PCBs.

5. Tilt out control panel slightly by pulling on two knobs on opposite sides.

6. Then pull gently upward. (If the panel is pulled forward too much, it will lock.)

7. Cables are still attached to the panel. Rest it vertically on the keys.

8. Disconnect all cables to the control panel except the one which is tie-wrapped to PCB 1 (not used in some earlier models). Disconnect this one from J302 and remove the control panel (to a safe place).

1/2.6 UNMOUNTING PCB 1 or 2

1. Remove control panel (see above).

2. Note that the back of the board is labelled with the control names, and the PCB board artwork for the component side is shown on pages 1/2.3 and 1/2.4. This should make it less necessary to remove a control panel board from the panel itself.

3. Pull off all knobs from the side to be removed.

4. Unscrew all potentiometer mounting nuts, using a nut driver to prevent scratching the lettering on the panel.

5. Unscrew the five or six screws which hold the board to its standoffs.

6. Tilt the board away from the panel (it is still soldered to the other board by ribbon cables).

7. When replacing a control panel board, check that every switch operates freely, before tightening all the pot nuts and mounting screws.

1/2.7 REMOVING SIDE PANELS

This must be done before either the wheel or end box can be removed.

1. Remove top panel (see page O.20).

2. Raise boards (see page O.21).

3. Remove the control panel (see page 1/2.12).

4. Remove the two screws in each side panel.

5. On the inside of both chassis sides there are two cable harnesses attached with hex-head screws. Remove all four screws. It will be necessary to use a 1/4" ratchet socket handle.

1/2.8 REMOVING WHEEL BOX AND END BOX

To remove the keyboard, the wheel box must first be removed.

1. Remove top panel (see page O.20).

2. Raise boards (see page O.21).

3. Remove the control panel (see page 1/2.12).

4. Remove side panels (see above).

5. To detach the wheel box, remove two screws through the side plate and two through the bottom panel.

6. To detach the right end box, remove two screws through the side and three through the bottom.

1/2.9 WHEEL SERVICE PROCEDURE

If you look carefully at the wheel box before disassembling it, you'll notice that the tops of the wheels are not exactly flat, but angled down at the left for finger comfort and better control. Obviously, when repairing a wheel, check that you do not put the wheel on backwards.

When the PITCH wheel is repaired, the wheel position on the pot shaft must be adjusted. Loosen the set screw and rotate the wheel (only) to its center detent position. Measure the voltage at the wiper of R1 (see schematic, page 1/2-2). While holding the wheel itself centered, use a small screwdriver to adjust the wiper for a 2.5-V reading. (This setting is not very critical, because the software initialization corrects for electro-mechanical error.) Then tighten the set screw (making sure the wheel does not rub against its slot). Initialize wheel (see page 1/2.6).

If repaired, the MOD wheel should be positioned so that when the wheel is at the bottom of travel, the wiper is grounded.

1/2.10 PCB 1 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-292	MOD WHEEL ASSEMBLY
J6	Wheel cable connector	J-056	5-PIN HOUSING
		P-031	POLARIZING PIN
		P-049	SOCKET PINS
R1/2	PITCH/MOD Pots	R-207	100K LINEAR POT
		Z-270	PCB 1 Assembled

1/2.10.1 INTEGRATED CIRCUITS

U101 Analog Regulator I-403 78L05CZ

The whole Multiplexer circuit, and ADC reference operates from a +5V analog supply created by U101. This is a 1% precision regulator which guarantees that the POT MUX reference voltage is at least 4.95V. This supply goes to PCB 2 over pin 1 of TB105.

U102 Mux Address Latch I-227 4042 QUAD LATCH

The clock input is normally high. When CSO16H returns low, four lower bits are transferred from the D inputs to the Q outputs. These are the Multiplexer addresses which encode a channel selection for each 16-channel multiplexer chip. (So if this chip is bad, the whole multiplexer may fail.) The addresses feed U109, and cross over to PCB 2. They also run to each of the pressure multiplexers on PCBs 10-14. R104 is for matching "HC" to "CMOS" logic levels.

U103 Mux Strobe Decoder I-246 4515

U103 decodes eight strobes which enable (low) the multiplexer ICs. Pin 1 is normally pulled high by R104. When CSO16H goes low the last data input prior to the transition is decoded and appears at outputs S0-7. For example, when D0-3 are 1010, I5 goes low, enabling the "middle" IC in the pressure multiplexer, U1201.

U104 Switch Input Driver I-257 74HC244

Pull-down array RA101 keeps the inputs to Driver U104 from floating high. -CSI02H then enables it to place on the Main Data Buss data representing closed switches in the column currently strobed by the matrix decoder (U110). Switch data from PCB 2 also connects to this Driver.

U105 LED Source Latch I-260 74HC374

Bits representing LEDs to be lit in one column are latched off the data buss by U105, when clocked by -CSO10H. C130 cleans up any ringing on the clock pulse caused by the long cable from PCB3. The latched bits turn on the transistors in array QA101 (plus Q101). RA102 limits drive current. Only the LEDs in the column currently decoded by U110 or U112 and inverted by U111 or U113, will light. These bits also drive portions of the LED Matrix appearing on PCB 2.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U106 ADC Input Driver I-257 74HC244

When -CSI06H goes low, this chip transfers the conversion data from the ADC over to the Main Data buss.

U107-4 ADC Reference I-303 1458 DUAL OP AMP

Because of the ratio of R111/R110, the ADC Vref is 97.6% of the +5Va supply which powers the pots. This guarantees that pot voltage reaches the ADC reference, for full conversion.

U107-7 Vmux Summer I-303 1458 DUAL OP AMP

Vmux from the eight multiplexers is summed by U107-7. R108 fixes the input impedance and holds Vmux near ground when the multiplexer is not enabled. R124/25 add a slightly negative voltage to overcome offset variations in the ADC and op amp, which ensures that ADC conversion starts at 00H.

Typical Vmux waveform:

Figure 1/2.10.1.1 **V: 1V/div**
VMUX, PITCH WHEEL CENTERED **H: 50 us/div**

U108 Analog to Digital Conv I-507 AD7574 ADC

The ADC converts the voltage of the pot selected by the multiplexer (Vmux), into an eight-bit number. It starts conversion whin the processor executes an input from port 07H (CSI06H low and AM0 high). Althogh -BUSY is not used in this system, it can be observed going low at this time and staying low for about 18 microseconds. Sometime after this the processor reads the data by inputting from port 06H (CSI06H and AM0 low). C107/R112 set the clock frequency of the converter.

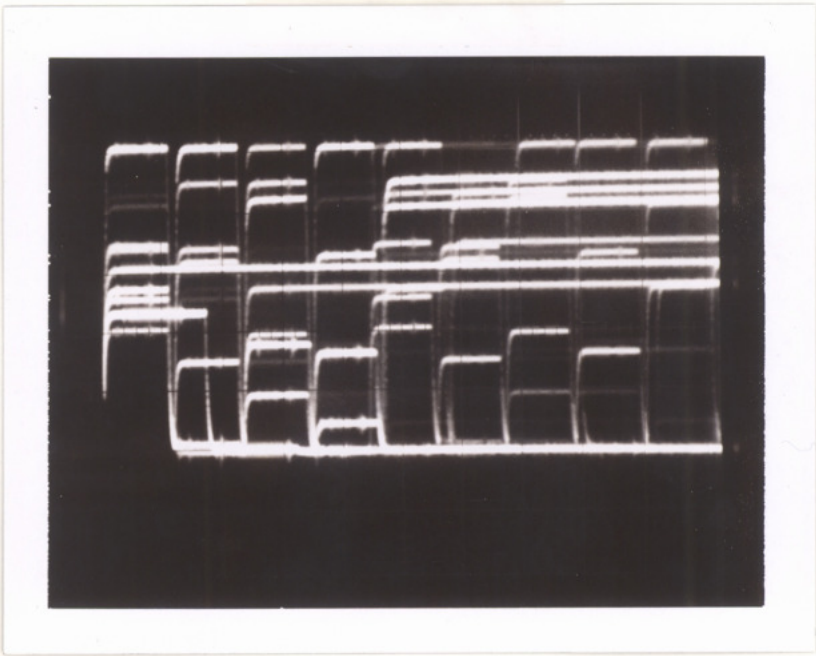


Figure 1/2.10.1.1

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U109	Multiplexer 0	I-245	MC14067 (4067)

U109 multiplexes most knobs on PCB 1, plus a few on PCB 2, and the wheels. The wheels are operated from +15V to ensure they can deliver the full 0 to 5V range to the ADC when operated through their limited rotation (about 120 degrees). R101 and R102 fine-tune this range. R115/C122 and R114/C123 filter wiper noise. D135 and D136 clamp the wheels to not exceed a few hundred millivolts above U109's supply voltage, protecting the chip. R116 on the multiplexer output is another protection against high currents which can result if two knobs set to different potentials are momentarily connected during power-up or -down.

U110	Matrix Column Decoder	I-218	4514 4-16 DEMUX

+CS012 latches four-bit numbers to decoder U110. Outputs 0 through 8 strobe the LED matrix columns. When one of these goes high, the inversion turns on LEDs which have been forward-biased by one of the transistors. Outputs 9 through 15 strobe the Switch matrix columns. When a column is decoded, any switches in that column which are closed, will route the high signal to an input of U104. The diodes wired throughout the switch matrix allow n-switch rollover--the pressing of any combination of switches--by isolating each switch. If the diodes were not present, signals from closed switches would return through other closed switches on that row, to pull other columns high.

A typical strobe signal:

Figure 1/2.10.1.2 **V: 1V/div**
CONTROL STROBE (U110-11, O0) **H: 50 us/div**

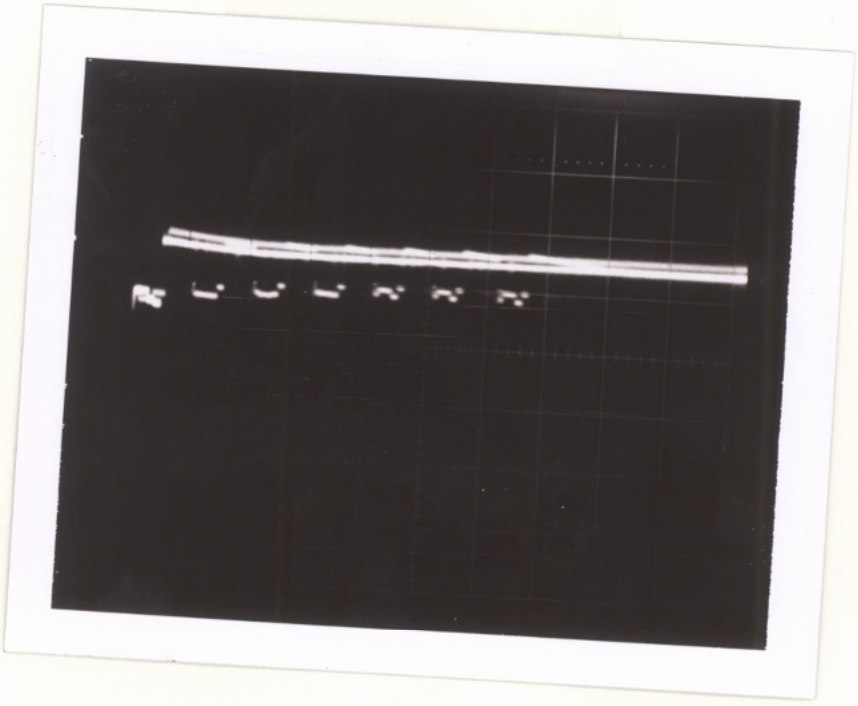


Figure 1/2.10.1.2

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U111	Led Matrix Sink Inverts decoder signal, and sinks LED current.	I-235	MC1413 (ULN2003)
U112	Led Column Latch This latch provides two additional column strobe signals for the LED matrix, when -CS014H returns high.	I-205	4013 DUAL FLIP-FLOP
U113	Led Matrix Sink See U111.	I-235	MC1413 (ULN2003)

1/2.10.2 **OTHER PARTS**

C101/02		C-020	1.0 25V 20% TANT RADIAL
C103-07		C-045	.1 50V 20% MONO RADIAL
C108		C-012	.01 50V 10% MYLAR RADIAL
C109		C-045	.1 50V 20% MONO RADIAL
C110		C-004	100 pF 50V 10% DISC RADIAL
C111-21		C-045	.1 50V 20% MONO RADIAL
C122/23		C-019	.47 35V 20% TANT RADIAL
C124-29		C-045	.1 50V 20% MONO RADIAL
C130		C-049	150 pF 1KV 10% DISC RADIAL
D101-34		D-005	1N914
D135/36		D-008	1N34
DS101-34	LEDs in S101-34	L-002	
J101		J-007	16-PIN DIP SOCKET
P101	Power Input	P-042	6-PIN PLUG PC
P102	Wheels	P-069	5-PIN LOCKING
P103	Pressure	P-081	13-PIN HEADER
Q101	LED Buffer	T-002	2N3904
QA101	LED Buffer	T-011	CA3082 TRANSISTOR ARRAY
R101/02		R-028	470K
R103		R-235	10K POT NYLON SHAFT
R104		R-010	2K
R105-07		R-235	10K POT NYLON SHAFT
R108		R-029	1M
R109		R-018	47K
R110		R-110	100K, 1%
R111		R-133	97.6K, 1%
R112		R-041	150K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R113		R-235	10K POT NYLON SHAFT
R114/15		R-012	10K
R116		R-008	1K
R117-23		R-235	10K POT NYLON SHAFT
R124		R-041	150K
R125		R-008	1K
RA101		R-305	3.9K x 8 RES ARRAY
	In some early (Rev B) units, this array was fashioned from discrete resistors and kludged to the board.		
RA102		R-300	39 x 8 RES ARRAY
S101-29	Programmable Switches	S-028	BLACK SRL LED
S130	Control Switch	S-029	GREY SRL LED
S131	Programmable Switches	S-028	BLACK SRL LED
S132	Control Switch	S-029	GREY SRL LED
S133	Programmable Switches	S-028	BLACK SRL LED
S134	RECORD switch	S-030	ORANGE SRL LED
		J-041	18-PIN DIP SOCKET
		PC1008-1	PCB 1
		Rev B required mods in ADC and TUNE LED. Rev C, no mods.	

1/2.11 PCB 2 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-271	PCB 2 Assembled

1/2.11.1 INTEGRATED CIRCUITS

U201	Multiplexer 1	I-245	MC14067 (4067)

Selects one of 16 pots on PCB 2. The ABCD address inputs and I1 come from a latch and decoder on PCB 1.

U202	Multiplexer 2	I-211	4051 1-8 MUX

As an eight-input device, the 4051 needs only three of the four available MUX lines.

The MASTER VOLUME and BALANCE knobs are not multiplexed. Instead they are wired to the audio output circuitry on PCB 6, via cable W3.

1/2.11.2 OTHER PARTS

C201-21		C-045	.1 50V 20% MONO RADIAL
D201-17		D-005	1N914
DS201-17	LEDs in S201-17	L-002	LED
DS218/19		L-005	DUAL DISPLAY
P201		P-067	6-PIN LOCKING
R201-10		R-235	10K POT NYLON SHAFT
R211		R-008	1K
R212-20		R-235	10K POT NYLON SHAFT
R221		R-008	1K
R222-25		R-235	10K POT NYLON SHAFT
S201-11	Control Switch	S-029	GREY SRL LED
S212	Programmable Switches	S-028	BLACK SRL LED
S213-17	Control Switch	S-029	GREY SRL LED
TB201		E-135	2" 8-WIRE JUMPER
TB202		E-136	2½" 8-WIRE JUMPER
TB203		E-139	2" 7-WIRE JUMPER
TB204		E-140	2½" 7-WIRE JUMPER
TB205		E-137	4" 7-WIRE JUMPER
TB206		E-138	4½" 7-WIRE JUMPER

The jumpers are all considered part of Z-271.

PC008-2B	PCB 2

Rev B silkscreen says "Rev A".

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
	PROGRAM Windows (2)	M-002	1.5" x 2" RED PLEXI
	Progammable Knobs	M-396	LOW-PRO KNOB BLK
	Non-Prog. Knobs	M-400	LOW-PRO KNOB SILVER
	Wheel	M-352	MOLDED WHEEL
	PITCH wheel detent	M-073	TENSION CLIP
	Panel Bottom Edge (3.5')	M-159	3/16" WIDE FOAM TAPE
		M-204	PITCH WHEEL BRACKET
		MW000-1	MOD WHEEL BRACKET
		MW1008-2	CONTROL PANEL
		MW1008-6	WHEEL BOX
	For wheels	M-070	6-32 x 1/2" SET SCREW
	Control Mounting	M-152	POTENTIOMETER NUT
		M-473	SCREW BLACK FLATHEAD 6-32 x 1/4 inch
	Upper control panel edge	M-025	BLACK FLATHEAD PHIL 6-32 x 5/16"

SCHEMATIC
sheet S
SD008-15
50% reduction
11x17
Black Line

PCB 15 DESIGNATOR MAP
PP008-15
1:1
11 x 17
Top layer Black line/Black screen
Bottom layer Blue screen

15.1 PRECAUTIONS

Before repairing the power supply, disconnect all of the PCBs from it.

To unmount PCB 15, remove six screws through the back panel. When installing, apply heatsink thermal compound where heatsinks contact the back panel.

After any repair, check that the regulator cases are not grounded to the chassis (use ohmmeter). Verify all voltages before reconnecting PCBs.

15.2 POWER SUPPLY TRIM

For trimming, the power supply must be fully loaded.

1. Measure -15V at TP1503 (e.g., -14.94V).

2. Measure +15V at TP1502 and adjust R1506 for equivalent positive reading (e.g., +14.94V).

3. Measure +5V at TP1505 (e.g., +4.96V).

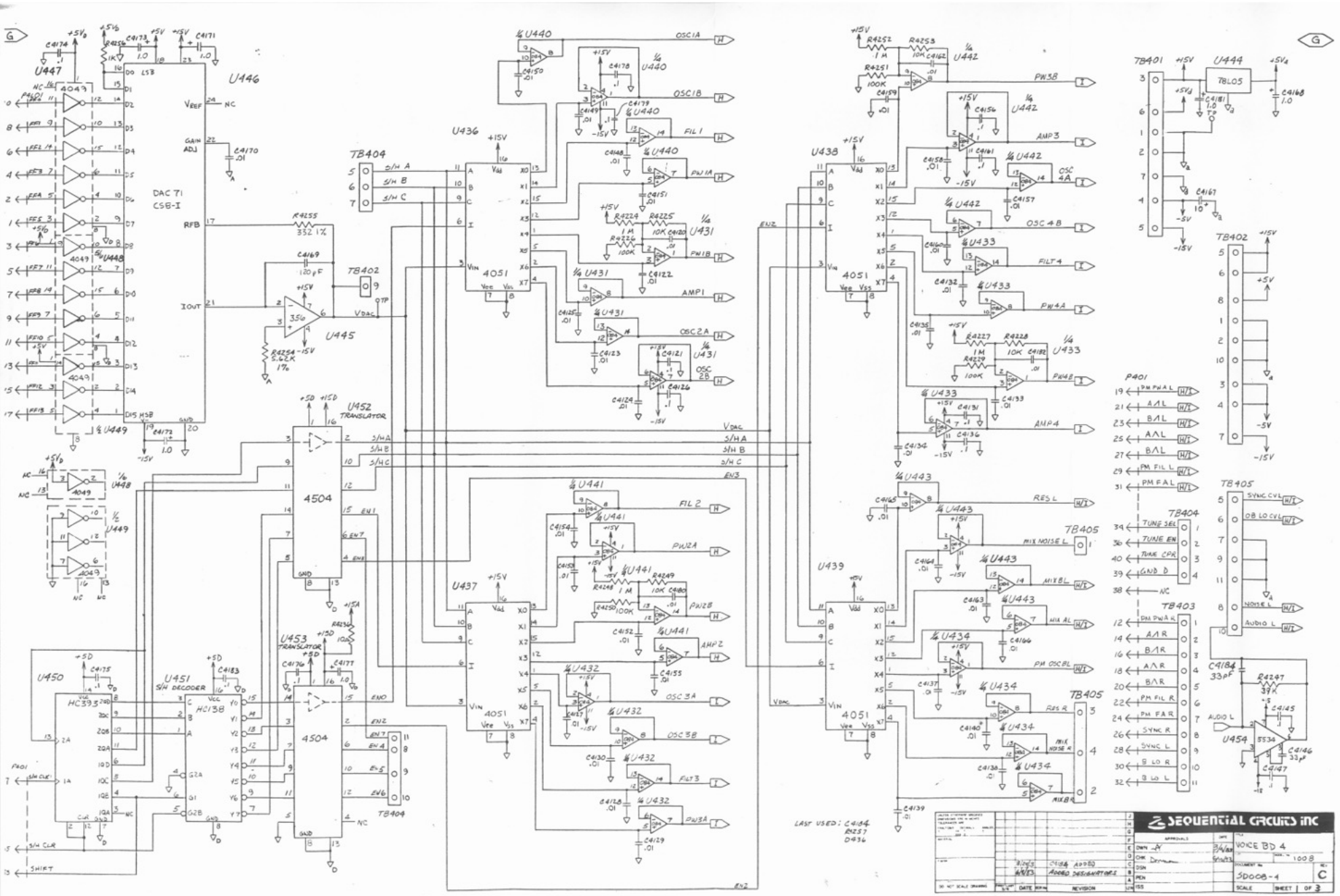
4. Measure -5V at TP1504 and adjust R1503 for equivalent negative reading (e.g., -4.96V).

15.3 HARDWARE DESCRIPTION

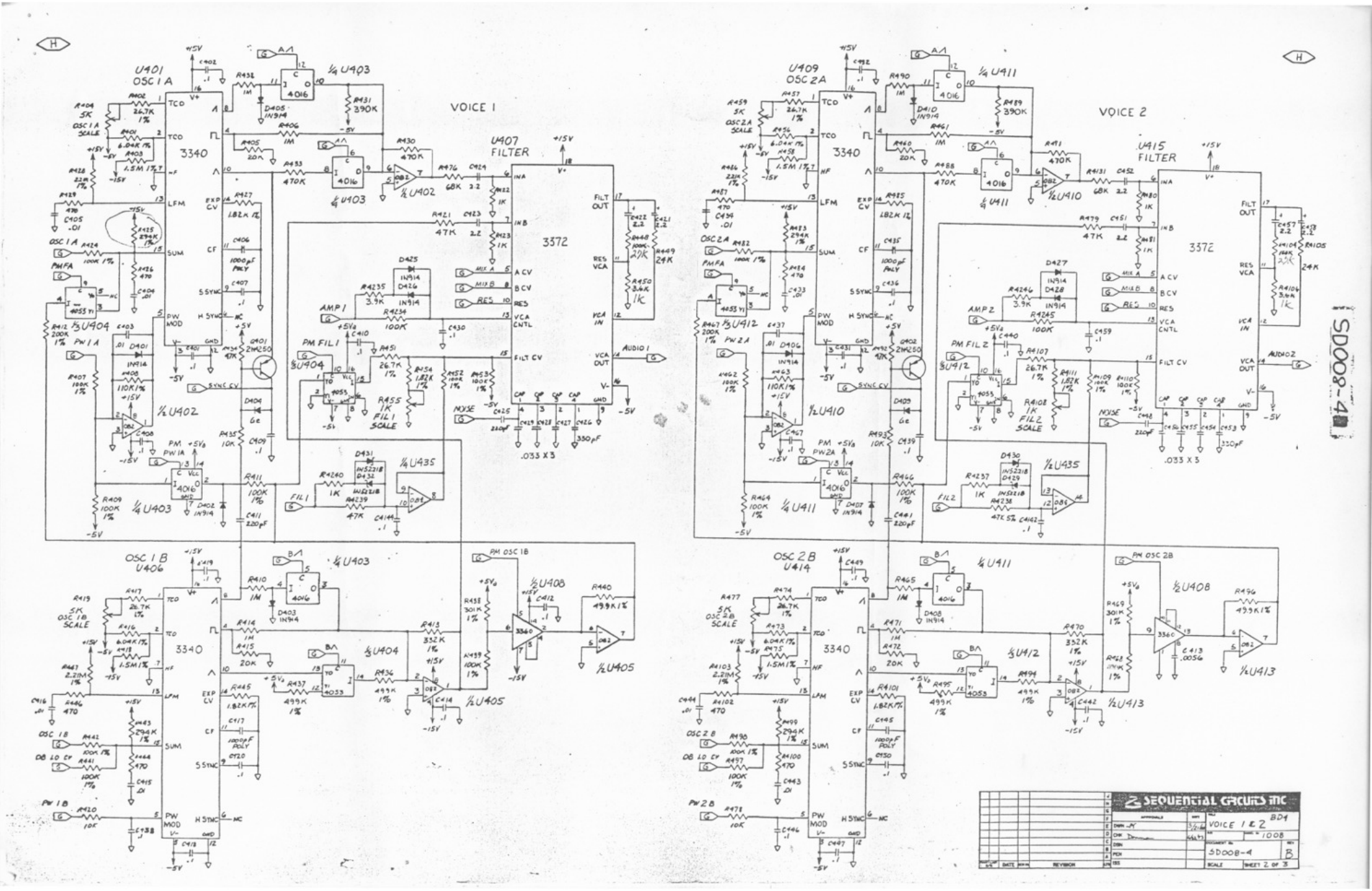
DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
15.3.1	**CHASSIS**		
F1	Fuse		
	Used in 115V models.	E-051	3/4A SLO-BLO
	Used in 230V models.	E-019	1/2A SLO-BLO
J2	Trans Secondary Conn	J-040	6-PIN JACK
	For J2	P-028	GOLD SOCKET CONTACTS
P1/J1	Power Cable	E-086	POWER CORD
P2	Power Receptacle	P-073	AC CONNECTOR
S1	Power Switch	S-025	POWER SWITCH LIGHTED
S2	Line Voltage Switch	S-062	110/220 VOLT SELECT
T1	Power Transformer	E-113	PWR TRANS
	A low-voltage secondary is provided to reduce heat of the 5-V regulators (which would result if they were driven from the 36V secondary).		
		E-128	FUSEHOLDER BODY
		E-129	FUSEHOLDER CAP (US)
	Power chassis ground	M-020	#10 LUG, 12 AWG
		Z-291	TRANSFORMER SUBASSY
		Z-274	PCB 15 ASSEMBLY
15.3.2	**INTEGRATED CIRCUITS**		
U1501	+5V Regulator	I-419	7805K or LM340K
	Powers PCB 3 computer, DAC and S/H decoder, PCB 6 MIDI hardware, and the switch and LED matrices on PCBs 1/2. Mounts on heatsink with M-371 insulator.		
U1502	-12V Regulator	I-415	79M12
	Powers only the four FIFO ICs (U361-64).		
U1503	-15V Regulator	I-408	79M15
	Powers the op-amps and analog synth ICs on PCBs 4 and 5, and audio output on PCB 6. Mounts on heatsink with M-370 insulator.		
U1504	-5V Regulator	I-420	LM337T ADJ
	Powers VCAs on PCBs 4/5 and 6. Mounts on heatsink with M-370 insulator.		
U1505	+15V Regulator	I-412	LM317T
	Powers the op-amps and analog synth ICs on PCBs 4 and 5, and audio output on PCB 6. Mounts on heatsink with M-370 insulator.		

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
15.3.3		**OTHER PARTS**	
C1501		C-089	6800, 25V ELECT AXIAL
C1502-04		C-076	2200, 35V ELECT AXIAL
	Secure C1501-04 to board with M-408 tie wrap.		
C1505/06		C-020	1 25V 20% TANT RADIAL
C1507		C-045	.1 50V MONO RADIAL
C1508/09		C-020	1 25V 20% TANT RADIAL
C1510		C-036	10 25V 20% TANT RADIAL
C1511		C-020	1 25V 20% TANT RADIAL
C1512		C-036	10 25V 20% TANT RADIAL
C1513/14		C-045	.1 50V MONO RADIAL
D1501-04	Low-Voltage Bridge	D-004	MR501/1N5401 100V 3A
	Supplies low-voltage regulators. When C1501 fully charges, Vunreg overrides the Vnv battery supply (on PCB 3) to provide the Program and Sequence NV RAM with full operating voltage.		
D1505-08	High-Voltage Bridge	D-004	MR501/1N5401 100V 3A
D1509/10	Power Detector	D-005	1N914
	When power is switched on, this rectifier extracts the turn-on transient (Vpd) which operates the computer reset circuit.		
P1501/02		P-042	6-PIN AMP HEADER
P1503-05		P-045	9-PIN AMP HEADER
R1501		R-125	121, 1%
R1502		R-156	243, 1%
R1503	-5V Trim	R-219	200 TRIMMER
R1504		R-157	2.55K, 1%
R1505		R-156	243, 1%
R1506	+15V Trim	R-219	200 TRIMMER
R1507		R-025	100K
	Forms a divider with R303, so Vpd is half of its rectified value.		
TP1501	-12V Test Point		
TP1502	+15V Test Point		
TP1503	-15V Test Point		
TP1504	-5V Test Point		
TP1505	+5V Test Point		
	(Rev A had no test points)		
	Two used	M-434	STANDOFF 6-32 x 1 3/8"
		M-099	4-40 NUT
		M-370	TO-220 INSULATOR
		M-371	TO-3 INSULATOR
		M-383	#4 STARWASHER
	Holds C1501-04	M-408	TIE-WRAP
	Heatsink spacers	M-425	PHENOLIC SHLDER WSHR
		M-428	4-40 X ½ PAN HEAD PHILLIPS
	Two used	MW1008-9	HEATSINK
		PC1008-15	POWER SUPPLY PCB
		Rev B silkscreen still says "Rev A".	

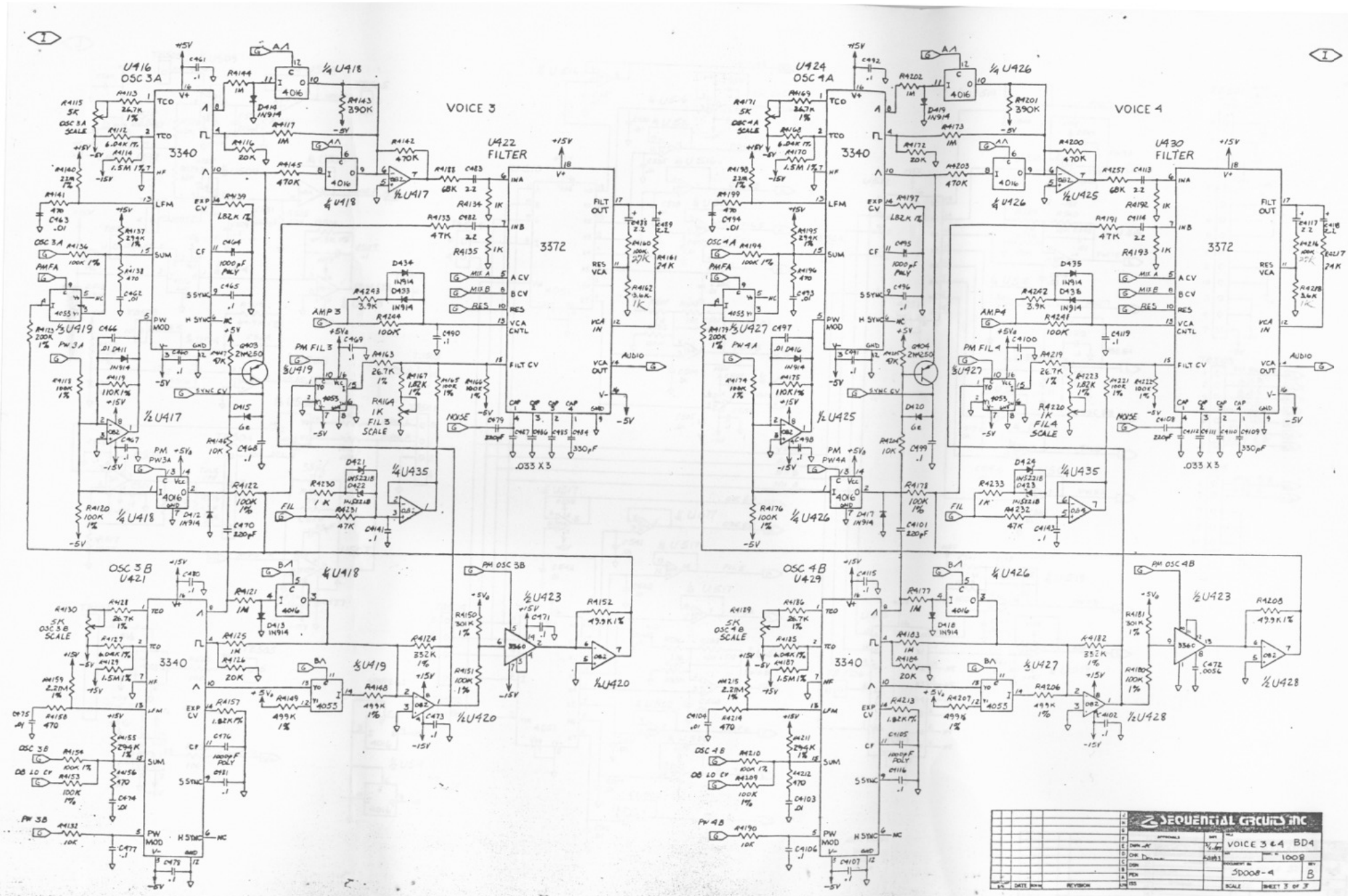
Schematic G
SD008-4 1/3
reduction 50%
11 X 17
Black line


SD008-4
SEQUENTIAL CIRCUITS INC
VOICE BD 4
SD008-4
C
SCALE
SHEET 1 OF 3
DAC 71
CSB-I
U446
U447
U445
U452
TRANSLATOR
U453
TRANSLATOR
U451
S/H DECODER
U450
U436
U437
U438
U439
U440
U441
U442
U443
U444
U445
U454
4504
4051
4049
TB401
TB402
TB403
TB404
TB405
P401
OSC1A
OSC1B
FIL1
PW1A
PW1B
AMP1
OSC2A
OSC2B
FIL2
PW2A
PW2B
AMP2
OSC3A
OSC3B
FIL3
PW3A
PW3B
AMP3
OSC4A
OSC4B
FILT4
PW4A
PW4B
AMP4
RES L
MIX NOISE L
MIXBL
MIX AL
PM OSCBL
RES R
MIX NOISE R
MIXBR
VDAC
S/H A
S/H B
S/H C
EN3
EN2
LAST USED: C4184 R4257 D436
ADDED DESIGNATORS

Schematic H
SD008-4 2/3
reduction 50%
11 X 17
Black line


VOICE 1
VOICE 2
U401 OSC 1A
U406 OSC 1B
U409 OSC 2A
U414 OSC 2B
U407 FILTER
U415 FILTER
3340
3372
OSC 1A SCALE
OSC 1B SCALE
OSC 2A SCALE
OSC 2B SCALE
PW 1A
PW 1B
PW 2A
PW 2B
PM FIL 1
PM FIL 2
AMP 1
AMP 2
FIL 1 1K SCALE
FIL 2 1K SCALE
.033 X3
SYNC CV
NOISE
AUDIO 1
AUDIO 2
SEQUENTIAL CIRCUITS INC
VOICE 1 & 2
5D008-A
SHEET 2 OF 3

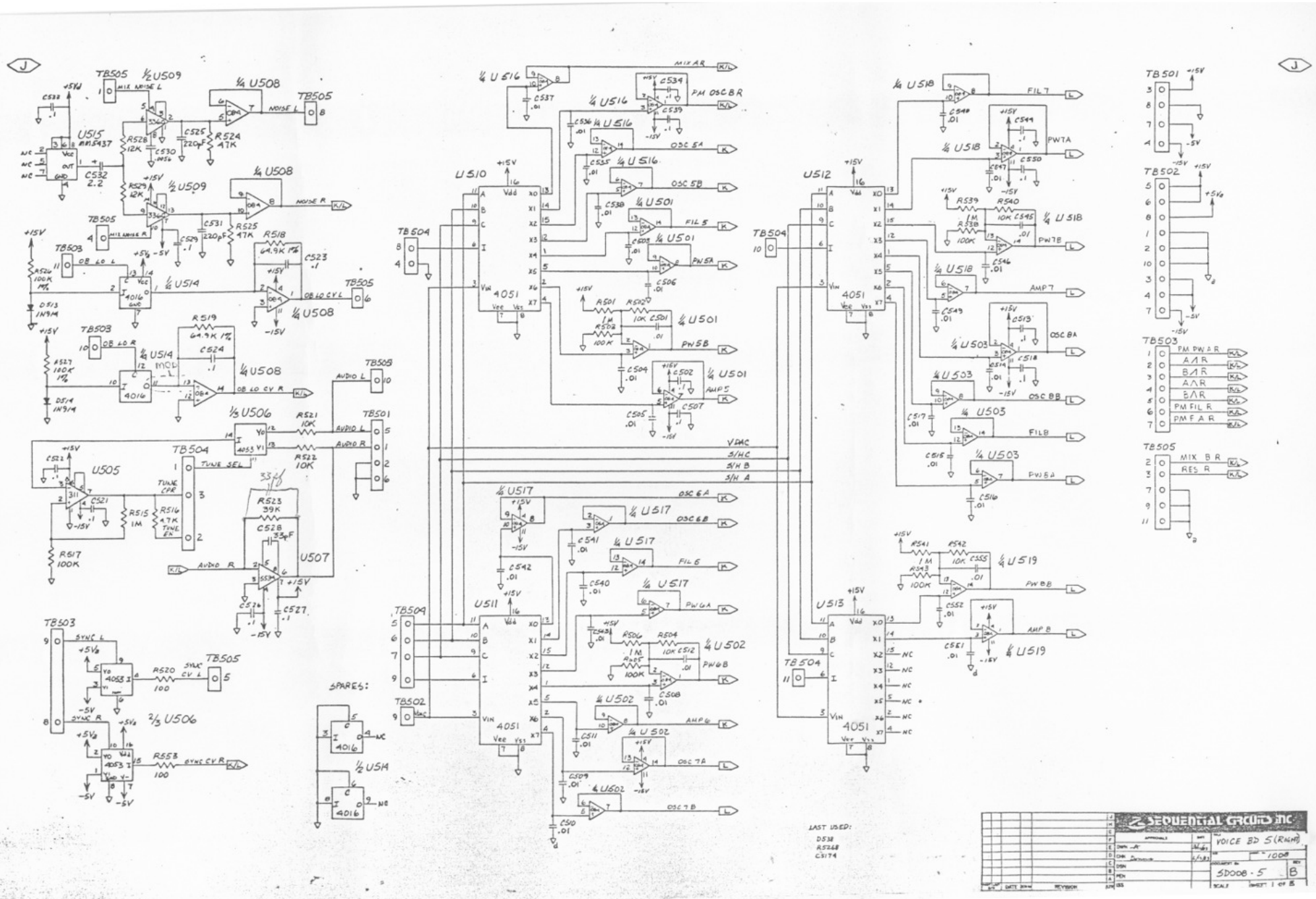
Schematic I
SD008-4 3/3
reduction 50%
11X17
Black line


VOICE 3
VOICE 4
U416 OSC 3A
U424 OSC 4A
U422 FILTER
U430 FILTER
3340
3372
OSC 3B U421
OSC 4B U429
SD008-4
SEQUENTIAL CIRCUITS INC
VOICE 3 & 4 BD
SD008-4
SHEET 3 OF 3

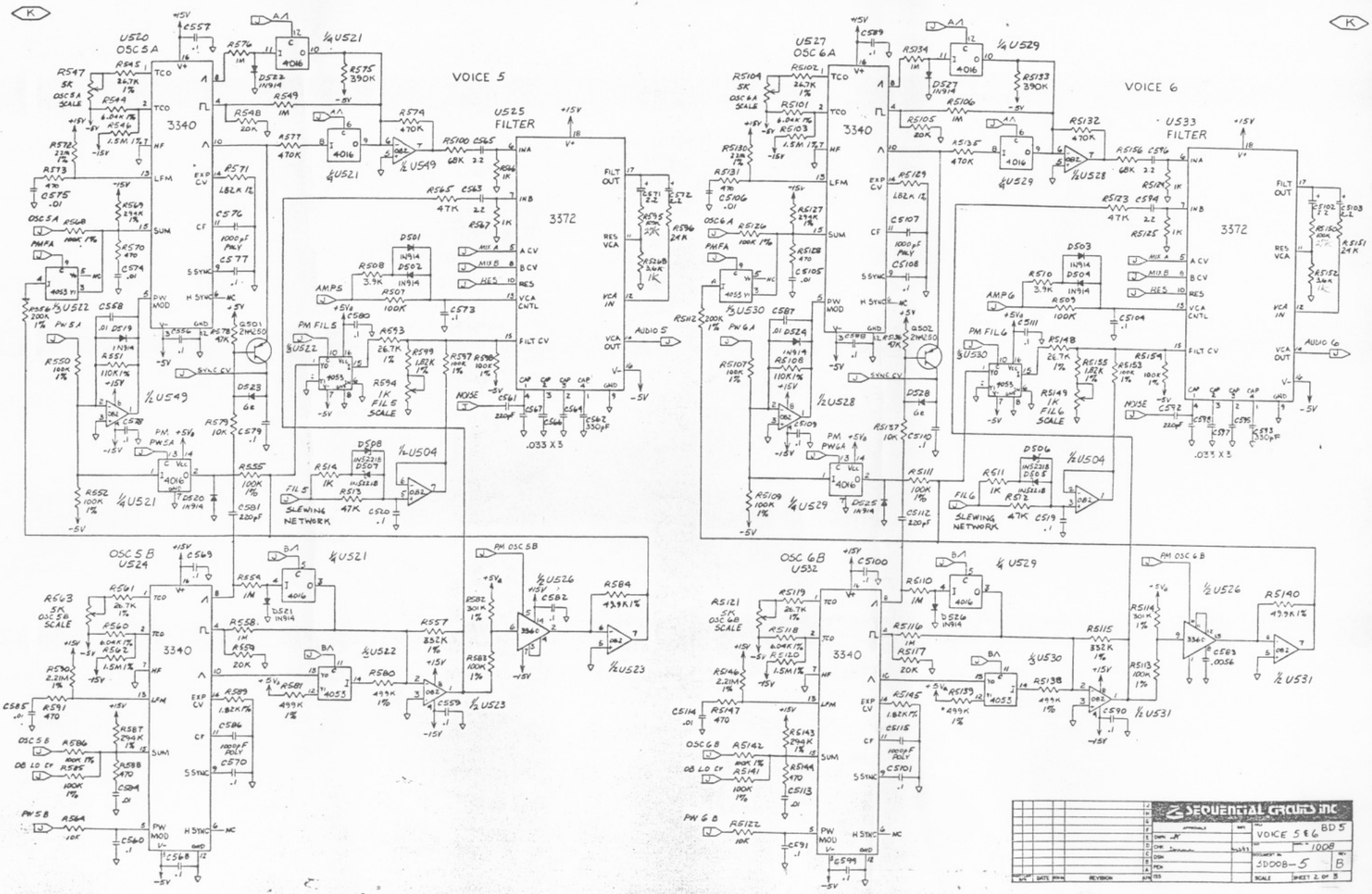
PCB 4 desig map
PP008-4
reduction 50%
11 X 17
2 color
Top layer black line/black screen
Bottom layer Blue screen

PCB 5 Desig Map
PP008-5
reduction 50%
11 X 17
2 color
Top layer black line/black screen
Bottom layer Blue screen

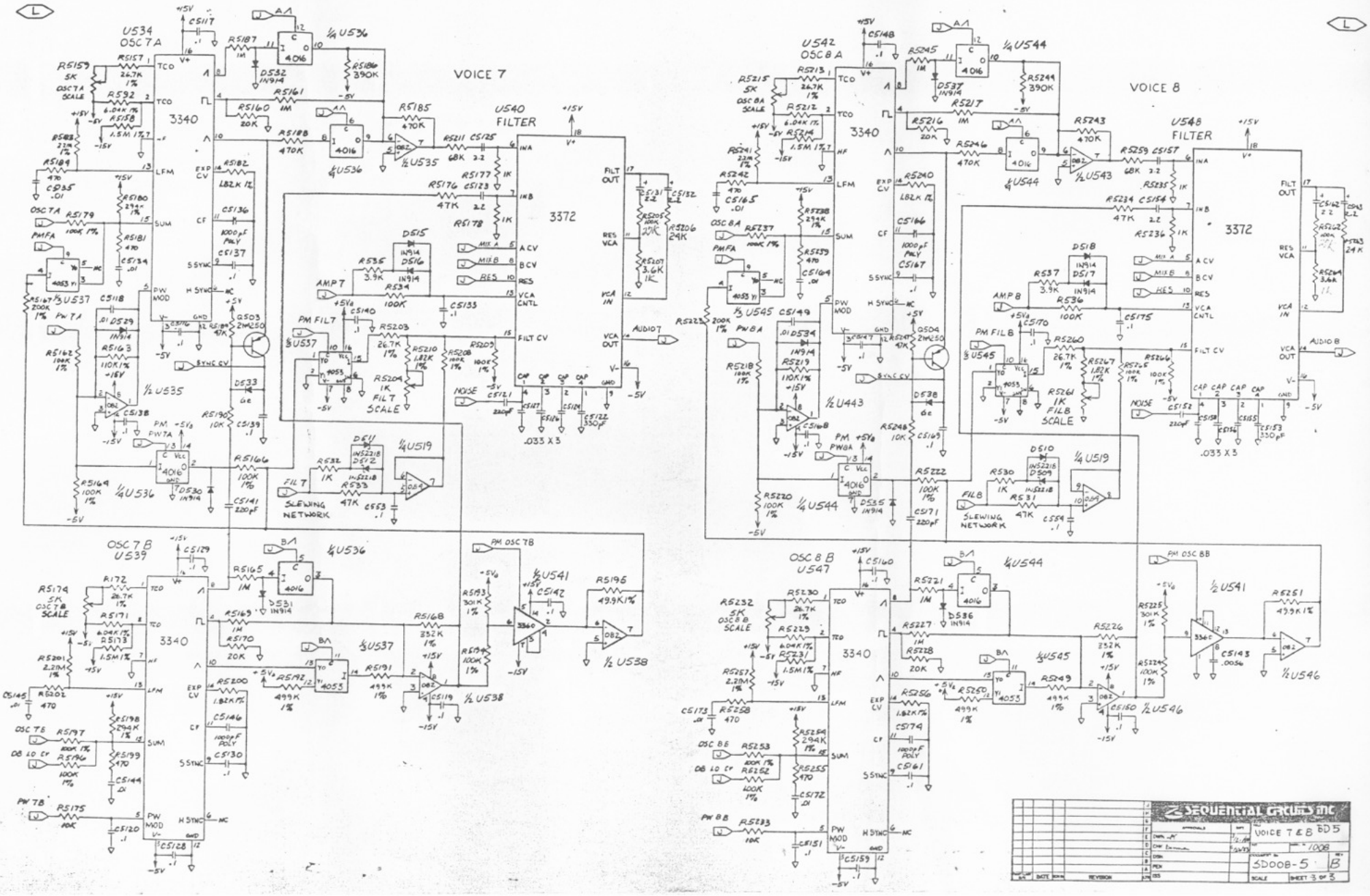
Schematic J
SD008-5 1/3
reduction 50%
11 X 17
Black line


TB505
½U509
¼U508
U515
MM5437
NOISE L
NOISE R
MIX NOISE L
MIX NOISE R
TB503
OB LO L
OB LO R
OB LO CV L
OB LO CV R
¼U514
4016
1N914
TB504
TUNE SEL
TUNE CPR
TUNE FR
U505
⅓U506
4053
AUDIO L
AUDIO R
TB501
U507
TB508
TB502
SYNC L
SYNC R
SYNC CV L
SYNC CV R
⅔U506
SPARES:
¼U516
¼U501
¼U517
¼U502
U510
U511
4051
PM OSC B R
OSC 5A
OSC 5B
FIL 5
PW 5A
PW 5B
AMP 5
FIL 6
PW 6A
PW 6B
AMP 6
OSC 7A
OSC 7B
VPAC
S/HC
S/H B
S/H A
U512
U513
¼U518
¼U503
¼U519
FIL 7
PW 7A
PW 7B
AMP 7
OSC 8A
OSC 8B
FIL 8
PW 8A
PW 8B
AMP 8
TB501
TB502
TB503
TB505
PM PW B R
A∧R
B∧R
A∨R
B∨R
PM FIL R
PM F A R
MIX B R
RES R
LAST USED:
D538
R5248
C5174
SEQUENTIAL CIRCUITS INC
VOICE BD 5 (REV H)
1008
SD008-5
B
SHEET 1 OF 5

Schematic K
SD008-5 2/3
reduction 50%
11 X 17
Black line


VOICE 5
VOICE 6
U520 OSC 5A
U527 OSC 6A
U524 OSC 5B
U532 OSC 6B
3340
U525 FILTER
U533 FILTER
3372
SEQUENTIAL CIRCUITS INC
VOICE 5 & 6 BD 5
5000B-5
B
SHEET 2 OF 3

Schematic L
SD008-5 3/3
reduction 50%
11 X 17
Black line


VOICE 7
VOICE 8
U534 OSC 7A
U542 OSC 8A
U539 OSC 7B
U547 OSC 8B
U540 FILTER
U548 FILTER
3340
3372
SEQUENTIAL CIRCUITS INC.
VOICE 7 & 8 BD5
5D00B-5
B
SHEET 3 OF 3

4/5.2 VOICE TESTING AND VOICE ASSIGNMENT

To test the eight individual voices, for each of the following tests you must play eight different keys. It is recommended that you use standard major scale fingering as a habitual way of always covering eight notes. Or you can use the sequencer.

All tests are performed by ear, the object generally being:

A. Smooth and continuous knob functions.

B. Clean switch functions.

C. Signal and modulation paths free of noise and distortion.

D. Consistency between the voices.

There will always be subtle differences between the voices. If not excessive, these non-uniformities help "warm" the Prophet's sound. (This is part of the point of using analog, as opposed to digital, tone generators and modifiers.)

Functional testing with the instrument closed should be thought of as research. The point is to bring out possible problems in the voices, and document them. When troubleshooting, it is better to use the LEFT and RIGHT audio outputs instead of MONO, because this will at least tell you which side may be involved. By listening to separate left and right outputs, you can narrow down a voice to one of four. You may be able to use the fact that following TUNE, in SINGLE mode the voices are assigned in the following order: 5, 6, 7, 8, 1, 2, 3, 4. In SPLIT or DOUBLE modes the order is 1/5, 2/6, 3/7, 4/8. Repeated notes are assigned to the same voice unless a newer note steals it. After the initial assignments it is difficult to predict the voice assignment.

Without opening the case and probing around on the voice boards it is not possible to identify with certainty which voice of the side is being played by which key. It will only be possible to identify with certainty which specific voice has a problem by opening the case. Then you can probe with an oscilloscope. But actually the easiest way to identify voices is to simply touch the VCO ICs with your finger, while holding the key to which the bad voice is currently assigned. The noise contributed by your finger will be very obvious in the audio output.

It is easy to troubleshoot individual voices by merely comparing either Left to Right, or between voices on the same side.

If all the Right voices seem intermittent, this can be caused by a PC trace along the front edge, near U507 Right Voice Summer, shorting to the support rail. The black anodizing wears off. This is fixed by adding some tape on the rail.

TUNING TEST

The first thing to do in response to tuning complaints is to make sure the owner knows to press the TUNE switch occasionally. And when everything seems transposed or out of tune, don't forget to check the owner's use of the PITCH wheel, MOD wheel, and MASTER TUNE. (It happens to everyone.)

If the -T8 only "plays out of tune in certain programs," this can be caused by owner programming in three basic ways:

First, because the filters are not tuned to the same accuracy as the oscillators, they don't perfectly tune in programs using them in resonance as tone sources.

Second, PRESSURE-, POLY-, or LFO-MOD may also introduce detuning modulation. To check this, switch off all modulation switches.

Third, the interval beween OSC A and B may not be correct, or OSC B may be detuned by its FINE knob.

Spend some time with the owner's machine to make sure these effects aren't coloring the -T8's performance.

Note: The actual tuning test is placed at the end of the functional test procedure because the -T8 must be on and operating in a relatively temperature-stable environment for about 25 minutes before critical tune testing or scaling can be attempted. During warm-up, press TUNE often (five-minute intervals or less). When the -T8 has stabilized, the time it takes for the TUNE routine will be fairly short. Once warmed-up, the -T8 has excellent stability.

1. Select the basic program (see page 4/5.9).

2. Initialize the PITCH wheel:

   a. Center the PITCH wheel solidly in its detent.

   b. While holding the RECORD switch, press PROGRAM/SEQUENCE 3. This writes the current wheel position into memory for reference in detecting changes in wheel position.

   c. Raise or lower the PITCH wheel, then return it to its center detent.

3. Press TUNE. If there is a noticeable "pop" in the audio, the software is Rev 3_3 (or lower) and needs to be updated.

4. Play the "A" key which lies under the number "4" in the PROGRAMMER section (A4), and check MASTER TUNE range, which should be +/- 1 semitone. To check range:

a. Center MASTER TUNE.
b. Play A. Remember pitch.
c. Turn MASTER TUNE to -5.
d. Play A#. Pitch should be approximately the same as A.
e. Center MASTER TUNE.
f. Play A. Remember pitch.
g. Turn MASTER TUNE to +5.
h. Play G#. Pitch should be approximately the same as A.

5. Switch A-440 on.

6. Playing the same A4, reduce MIXER OSC A level to about "4" to match A-440 tone and clarify slow "beating."

7. Center MASTER TUNE then tune for minimum beating.

Because MASTER TUNE is digitized, it may not be possible to remove <u>all</u> beating.

8. Switch A-440 off.

MASTER TUNE should now be positioned within the +/-1 dial marks of 0 center. If it had to be adjusted outside of this range to reach A-440, this indicates that the PITCH wheel may need to be reinitialized, or oscillator scaling needs to be performed (see page 4/5.31).

9. Play and listen to the tuning of various programs.

If all voices in a program seem wrong or somehow altered, suspect memory or the sample/holds. If one or occasional notes are bad, suspect one of the voices. A -T8 in need of scaling exhibits greater "beating" between voices, particularly as the PITCH wheel is rotated to its extremes.

10. If tuning is the main service problem, continue with functional testing while the instrument warms-up in preparation for later tuning testing or scaling. If there is other service to perform, leave scaling until last.

OSCILLATOR A FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. Press TUNE.

3. While playing, raise OSC A FREQUENCY gradually enough to be sure there are no missing semitones in its range.

> Note that it is normal for all knob ranges to operate from just below 2 on the dial to only 7 or 8. It is the range of functional control not physical range that is being tested.

4. Check that FREQUENCY range is four octaves.

> These occur at approximately "3," "4," "5½," and"6-3/4."

5. Set FREQUENCY to approximately 3.

> Tune A3 (under the LEFT switch) to A-440, if you like.

6. Switch sawtooth off and triangle on. This should yield a pure timbre, with no obvious distortion, but at a lesser volume than the sawtooth.

7. Switch triangle off and pulse on. This should be a full tone with no apparent distortion.

8. Adjust PULSE WIDTH and observe smooth change in timbre.

> At the extreme knob settings the pulses will "thin out" until they degenerate to dc, resulting in no audio output. Check that for each voice this point is about the same.

9. Return PULSE WIDTH to 5.

10. Switch SYNC on. While rotating OSC A FREQUENCY through its range, listen for timbral sweep. Switch SYNC off.

11. Switch off pulse (so no waveshapes are on).

12. Increase monitor to high level to check for bleed through.

13. Turn monitor level back down.

OSCILLATOR B FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. Switch OSC A sawtooth off.

3. Switch OSC B sawtooth on.

4. Raise MIXER OSC B to 10.

5. Activate TUNE.

6. Raise OSC B FREQUENCY gradually enough to be sure there are no missing semitones in its range.

7. Check that FREQUENCY range is four octaves.

8. Set FREQUENCY to approximately 3.

    Tune A3 (under the LEFT switch) to A-440 if you like.

9. Check that FINE has a one whole-tone range.

10. Switch sawtooth off and triangle on. This should yield a pure timbre, with no obvious distortion, but at a lesser volume than the sawtooth.

11. Switch triangle off and pulse on. This should be a full tone with no apparent distortion.

12. Adjust PULSE WIDTH and observe smooth change in timbre.

    At the extreme knob settings the pulses will "thin out" until they degenerate to dc, resulting in no audio output. Check that for each voice this point is about the same.

13. Return PULSE WIDTH to 5.

14. Switch off pulse (so no waveshapes are on).

15. Increase monitor to high level to check for bleed through.

16. Turn monitor level back down!

17. Switch pulse back on.

18. Switch LO FREQ on and play up and down the keyboard.

    This will convert the audio to low-frequency pulses which will increase in rate towards the higher end of the keyboard.

19. Switch KEYBOARD off, and vary OSC B FREQUENCY.

    The keyboard will now not increase the oscillator pitch.

20. Switch LO FREQ off, and vary OSC B FREQUENCY.

    The oscillator will now function as a fixed-pitch audio oscillator.

MIXER/NOISE FUNCTIONAL TEST

1. Select basic program (see page 4/5.9).

2. Rotate MIXER OSC A through its range several times, checking for smooth attenuation.

3. Set MIXER OSC A to 0.

4. Increase monitor to high level to check for VCAs which don't completely shut off.

5. Turn monitor level back down!

6. Switch OSC A sawtooth off.

7. Switch OSC B sawtooth on.

8. Rotate MIXER OSC B through its range, checking each voice for smooth attenuation.

9. Set MIXER OSC B to 0.

10. Increase monitor to high level to check for VCAs which don't completely shut off.

11. Turn monitor level back down!

12. Switch OSC B sawtooth off.

13. Rotate MIXER NOISE through its range, checking each voice for smooth attenuation.

14. Set MIXER NOISE to 0.

15. Increase monitor to high level to check for bleed-through.

16. Turn monitor level back down!

FILTER FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. Switch OSC A sawtooth off.

3. Set CUTOFF to 3.

4. For each voice, increase RESONANCE from 0 to 10.

   Playing near the middle of the keyboard, all eight filters should start to oscillate by 8 on the dial.

5. Turn RESONANCE to 10.

   All voices should have nearly equal volume and should track the keyboard in fairly good tune. If not, scaling may be needed (see page 4/5.32).

6. For each voice, adjust CUTOFF gradually throughout its range.

   Listen for smooth frequency control of the resonating filters.

   Return CUTOFF to 3.

7. Raise GLIDE to 7 and play at the ends to demonstrate that the slewed keyboard CV is controlling the filters.

8. Return GLIDE to 0.

9. While playing the keyboard, reduce KEYBOARD AMOUNT.

   The octave will gradually become detuned as the interval between notes decreases. When KEYBOARD AMOUNT is at 5 the filters will track in approximately quarter-tones.

10. Set KEYBOARD AMOUNT to 0.

    Now filter pitch is not affected by keyboard.

11. Return KEYBOARD AMOUNT to 10.

12. Turn CUTOFF to 0.

13. While playing, raise ENV AMT from 0 through 10.

    This will act like the cutoff knob.

FILTER ENVELOPE FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. Switch OSC A sawtooth off.

3. Set RESONANCE to 10.

4. Set CUTOFF to 0.

5. Set ATTACK to 6.

6. Set SUSTAIN to 0.

7. As the ENVELOPE AMOUNT knob is raised from 0 to 10, each keystroke should cause the filter frequency to shoot up, then snap back to its initial frequency.

8. Leave ENVELOPE AMOUNT set to 4.

9. Check the ATTACK range.

> When set to 0, attack is instantaneous. At 10, the attack takes 10 seconds. Note that since the envelopes are computed, they are not going to fail if the computer is running. Therefore you don't need to test each voice--only a failure with a knob or ADC will affect the envelopes.

10. Return ATTACK to 0.

11. Check smooth control of DECAY range, which is exhibited by a descending sweep.

12. Return DECAY to 0.

13. Observe that raising and lowering SUSTAIN smoothly controls the filter frequency.

14. Return SUSTAIN to 5.

15. Check the RELEASE range.

> Note: To hear the filter release, the amplifier release must be set to equal or longer duration.

16. Switch SECOND RELEASE on and off and check that the LED goes on and off.

17. Connect the footswitch to the 2ND RELEASE FOOTSWITCH jack.

    (If an official footswitch is not available, a jumper clip which momentarily connects tip to sleeve will work.)

18. Check footswitch operation of SECOND RELEASE.

    When the footswitch is pressed, the SECOND RELEASE LED will light.

4/5.2.7 AMPLIFIER ENVELOPE FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).
2. Check the ATTACK range, from 0 - 10.
3. Return ATTACK to 0.
4. Turn SUSTAIN to 0.
5. Check smooth control of DECAY range.
6. Set DECAY to 0.
7. Observe that raising and lowering SUSTAIN smoothly controls the voice amplitude.

   With ATTACK, DECAY, SUSTAIN all at 0 there will still be a slight transient.

8. Turn SUSTAIN to 5.
9. Check the RELEASE range.
10. Switch ADR on and off--see that the LED goes on and off.

LFO-MOD FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).

2. Set LFO FREQUENCY to 5.

3. Set INITIAL AMT to 5.

4. Switch FREQ A DESTINATION on.

   This will produce a heavy vibrato.

5. Check the FREQUENCY range.

6. Leave FREQUENCY set to 5.

7. Switch sawtooth on.

   The triangle will automatically switch off.

8. Check the range of the INITIAL AMT knob.

9. Switch square wave on.

   The sawtooth will automatically switch off.

10. Check that with INITIAL AMT at 10, the note played is "arpeggiated" at the octave.

11. Switch ENABLE WHEELS on.

12. Check that the MOD WHEEL has the same range as the INITIAL AMT knob.

    a. Set INITIAL AMT to 0.

    b. Use the MOD wheel. (Full range should be same as INITIAL AMT.)

    c. Return MOD wheel to the "off" position.

13. Switch ENABLE WHEELS off.

14. Turn INITIAL AMT to 5.

15. Switch the triangle on.

    The square wave will automatically switch off.

16. Listen again to the vibrato on OSC A.

17. Under LFO-MOD, switch FREQ A off.

18. Switch FREQ B on.

19. Switch OSC B pulse on.

20. Turn MIXER OSC A to 0.

21. Turn MIX OSC B to 10.

22. Check the vibrato applied to OSC B.

23. Check the range of INITIAL AMT.

24. Switch FREQ B off.

25. Switch PW on.

26. Check INITIAL AMT and FREQUENCY ranges of pulse-width modulation to OSC B.

27. Turn MIXER OSC B to 0.

28. Turn MIXER OSC A to 10.

29. Switch OSC A sawtooth off.

30. Switch OSC A pulse on.

31. Verify pw-modulation, using INITIAL AMT.

32. Switch off PW.

33. Switch FILTER on.

34. Lower CUTOFF to accentuate filter vibrato.

35. Check INITIAL AMT and FREQUENCY ranges of filter modulation.

4/5.2.9 POLY-MOD FUNCTIONAL TEST

4/5.2.9.1 FILT ENV SOURCE AMOUNT TEST

1. Select the basic program (see page 4/5.9).

2. Turn FILTER ENVELOPE ATTACK to 6.

3. Turn FILTER ENVELOPE DECAY to 6.

4. Turn FILTER ENVELOPE SUSTAIN to 0.

5. Switch on POLY-MOD FREQ A.

6. Check the range of FILT ENV.

   As it is rotated towards +5, the pitch will be swept further upward, then return to its basic pitch. When rotated to -5, the pitch sweeps negatively then returns.

   When FILT ENV is maximum, raising FILTER ENVELOPE SUSTAIN to maximum should demonstrate that the envelope sweeps OSC A across approximately one octave.

7. Return SUSTAIN to 0.

8. Switch FREQ A off.

9. Switch PW A on.

10. Switch OSC A sawtooth off.

11. Switch OSC A pulse on.

12. Check that FILT ENV applies pulse modulation.

    To get the feel of the pulse width modulation, adjust the PULSE WIDTH knob to its extremes. The point at which the pulse cuts out will change, depending on the state of the envelope.

13. Switch PW A off.

14. Switch FILTER on.

15. Switch OSC A pulse off.

16. Turn CUTOFF to 0.

17. Turn RESONANCE to 10.

18. Check range of FILT ENV +5/-5 applied to filter in resonance. The sweep range should also be about one octave in both directions.

4/5.2.9.2 OSC B SOURCE AMOUNT TEST

1. Reselect basic program (see page 4/5.9).

2. Turn OSC B FREQUENCY to 4.

3. Switch OSC B pulse on.

4. Switch OSC B LO FREQ on.

5. Switch POLY-MOD FREQ A on.

6. Check range of OSC B SOURCE AMOUNT.

   It should be able to drive OSC A to an octave. The individual voices should not vary by more than a semitone. Because KEYBOARD is on, the LFO rate accelerates according to key position.

7. Switch OSC B pulse off.

8. Turn OSC B SOURCE AMOUNT to 10.

9. Toggle the FREQ A switch to check there is no more than a semitone of offset.

10. Leave FREQ A off.

11. Switch PW A on.

12. Switch OSC A sawtooth off.

13. Switch OSC A pulse on.

14. Switch OSC B pulse on.

15. Turn OSC B SOURCE AMOUNT to 10.

16. Adjust OSC A PULSE WIDTH to the point where sound is cut off by the modulation.

17. Check the range of OSC B SOURCE AMOUNT modulation to OSC A.

    Each oscillator should cut out at approximately the same setting of OSC A PULSE WIDTH.

18. Switch PW A off.

19. Switch FILTER on.

20. Switch OSC A pulse off.

21. Turn CUTOFF to 0.

22. Turn RESONANCE to 10.

23. Turn FILTER SUSTAIN to 0.

24. Check range of OSC B modulation of filter frequency.

    It should be several octaves.

    The scaling of the filters is not totally accurate, so they will be somewhat out of tune.

25. Switch OSC B pulse off.

26. Turn OSC B SOURCE AMOUNT to 10.

27. Toggle the FILTER switch to check there is no more than a semitone of offset.

PRESSURE-MOD FUNCTIONAL TEST

Every key must be checked for proper pressure response. This is done by applying the pressure signal to bend oscilllator frequency, and listening for smooth and consistent pitch bending.

1. Select the basic program (see page 4/5.9).

2. Switch PRESSURE-MOD FREQ A on.

3. Switch A-440 on.

4. Hold the lowest key (A0), and tune OSCILLATOR A FREQUENCY to the A at approximately 5½ on the dial.

5. Switch A-440 off.

6. Starting at the bottom, check that for each key:

   a. There is a threshold between the point at which the key falls with normal velocity, and the actual engagement of the pressure sensor. In other words, with the key down but no more force applied than needed, there should be no pitch offset. (For threshold adjustment, see page K.8.)

   b. No key acts as a pressure "switch."

   c. Pressure bends each note by at least an octave, without needing excessive force.

   d. There are no jumps greater than a major third (three semitones) in the bending. To hear the jumps, you have to bend the note slowly.

7. When you get up to the center of the keyboard, return OSC A FREQUENCY to 0.

8. Identify any malfunctioning keys with tape or such. You'll need to note somehow whether the key has a threshold problem or a "jumpy" sensor.

9. After checking the pressure sensors, to check the PRESSURE-MOD destinations, first select the basic program (see page 4/5.9).

10. For each PRESSURE-MOD switch setting below, adjust the AMOUNT knob +/-5 to check the range.

11. Switch FREQ B on.

12. Switch OSC B pulse on.

13. Turn MIXER OSC A to 0.

14. Turn MIXER OSC B to 10.

15. Check range.

16. Switch FREQ B off.

17. Switch PW on.

    It should be possible to cut-off all voices near the same AMOUNT setting on both sides.

18. Switch PW off.

19. Switch FILTER on.

20. Turn MIXER OSC B to 0.

21. Adjust CUTOFF to 3.

22. Turn RESONANCE to 10.

23. Check the range.

24. Reselect basic program.

25. Switch AMP on.

26. Check AMP pressure range.

    When set to -5, pressure should be able to shut off all voices evenly.

27. Switch AMP off.

28. Switch LFO AMT on.

29. Turn LFO FREQUENCY to 5.

30. Turn INITIAL AMT to 3.

31. Switch LFO-MOD FREQ A on.

32. Check PRESSURE-MOD AMOUNT range.

When set to -5, modulation may be decreased to nothing with a certain amount of pressure. Adding more pressure will then increase depth again. The point at which this happens is determined by the INITIAL AMOUNT knob.

36. Switch LFO AMT off.

37. Switch LFO FREQ on.

38. Check pressure range on LFO FREQ.

Note: Computer diagnostics for examining the pressure sensing system are described in section 10-14.

VELOCITY FUNCTIONAL TEST

1. Switch PRESET on and select a suitable velocity program, such as Factory R11 (Piano) or R15 (Vibalimba).

2. Play all keys, first quickly, then slowly, and listen for consistency of response.

3. Identify any malfunctioning keys (with tape or such).

4. Select the basic program (see page 4/5.9).

5. Adjust AMP ENV PEAK from 0 to +5.

   This is the loudness sensitivity control. When set to 0 it doesn't matter how fast the key is pressed. When set to +5 the keyboard is maximally sensitive. Slow keystrokes play softly while fast ones play loudly.

6. Adjust AMP ENV PEAK from 0 to -5.

   When moved towards -5 the keyboard becomes inversely loudness sensitive. Slow keystrokes will play loudly while fast ones will be quieter. (In case you're wondering, this is used to mix programs in DOUBLE mode.)

7. Return AMP ENV PEAK to 0.

8. Turn CUTOFF to 0.

9. Turn ENV AMT to 10.

10. Adjust FILTER ENV PEAK from 0 to +5.

    This is the timbre sensitivity control. When set to 0 it doesn't matter how fast the key is pressed. When set to +5 the keyboard will be maximally sensitive. Slow key strokes will have a duller timbre while fast ones will be brighter.

11. Adjust FILTER ENV PEAK from 0 to -5.

    When moved towards -5 the keyboard will be inversely timbre sensitive. Slow key pressings will be bright while fast ones will be dull.

12. Reselect the basic program.

13. Set AMPLIFIER ENVELOPE ATTACK to 7.

14. Set AMPLIFIER ENVELOPE DECAY to 7.

15. Set AMPLIFIER ENVELOPE SUSTAIN to 0.

16. Hold a key and notice the amplitude rise then fall.

    This will take about five seconds, and is independent of the speed at which the key is pressed.

17. Adjust ATT/DEC ENV RATE from 0 to 10.

    Notice that as it is increased, playing faster accelerates the envelopes while playing slower lengthens them. When set to 10, the rates can be made quite short or quite long by touch.

18. Reselect the basic program.

19. Set AMPLIFIER ENVELOPE RELEASE to 5.

20. Play some keys and notice the rate at which the amplitude falls.

    This will take about one second, and is independent of the speed at which the key is released.

21. Adjust REL ENV RATE from 0 to 10.

    Notice that as it is increased, releasing faster accelerates the release time while releasing slower lengthens it. When set to 10, the release rate can be made quite short or quite long by touch.

Note: Computer diagnostics for investigating the optical sensing hardware are described in section 7-9.

4/5.3 SCALING PROCEDURE

Note: before proceeding, initialize PITCH wheel:

a. Center the PITCH wheel in its detent.

b. While holding the RECORD switch, press PROGRAM/SEQUENCE 3. This writes the current wheel position into memory for reference in detecting changes in wheel position.

c. Raise or lower the PITCH wheel, then return it to its center detent.

Note: Scaling is placed at this point in the functional test procedure because the -T8 must be on and operating in a relatively temperature-stable environment for about 25 minutes before this can be attempted. During warm-up, press TUNE often (five-minute intervals). When the -T8 has stabilized, the time it takes for the TUNE routine will be fairly short and constant. Once warmed, the -T8 has excellent stability.

Now that the Prophet-T8 has been thoroughly warmed up, it can be scaled. Oscillator and filter scaling is simplified through the use of a special routine which provides visual indication of correct adjustment. Each oscillator and filter has one trimmer for scaling during this routine. Turning each trimmer clockwise causes the TO TAPE LED to turn off. Turning each trimmer counterclockwise causes the LED to light. Correct scaling is acheived when the trimmer is set so the LED flickers or is either just on or off.

1. Switch power off.

2. Remove top panel (for instructions see page O.20).

3. Switch power on.

4. When tune routine is finished, hold A-440 and press TUNE to enter the Scaling routine.

5. All trimmers are "gooped" with a special removable compound (SCI# Q-60). Remove goop before making scale adjustments. When the scaling procedure is complete, regoop all trimmers.

6. Correct scaling adjustment is indicated when the TO TAPE LED just toggles from on-to-off, or off-to-on. When lit the TO TAPE LED indicates the trimmer should be turned clockwise, when off the LED indicates the trimmer should be turned counterclockwise.

7. Scale OSC 1A, OSC 1B, FILT 1, OSC 2A, ... To advance along this sequence, press TUNE.

There is no panel indication of where you are in the scaling routine. All oscillators which aren't being tuned are held down at a very low frequency. If an oscillator is active, therefore, you can see its output, with a scope on pin 8. To find an active filter, touch scope probe to top of the 2.2 uF electrolytics near pin 17. If this filter is active, you should see a sine wave.

8. After Filter 8 is scaled, press TUNE to start normal tune routine.

9. Press TUNE several times, until everything seems stable.

4/5.4 DAC AND SAMPLE/HOLD DIAGNOSTICS

These Z-8002 diagnostics reside within the standard operating system PROMs. There are three basic diagnostic tests plus fourteen tests which exercise each bit of the DAC. The tests are selected by momentarily (less than one second) grounding the Z-8002's NMI test point (located next to BREQ). Each ground tap advances to the next test. The only way to exit the routine is to reset by switching power off then back on. (If you unground the Z-80 BREQ, the -T8 will enter TUNE but not leave it.)

To activate Final diagnostics:

1. Switch power off.

2. Remove the top panel.

3. If Z-8002 was disabled for Z-80 test, unground the Z-8002 BREQ test point.

4. Disable the Z-80 by tying its BREQ (located just above it, U310) test point to ground. There is a GND test point in the center of the board. (With the Z-80 disabled, it doesn't matter which ROM--operation or DT8_4--is installed in the Main system. However for a complete check of Common RAM, $\overline{DT8_4}$ is used--see page 3.18.)

5. Switch power on. As the Main processor is effectively disabled, the control switches won't work. Disregard any lit LEDs.

6. The Final system is now in a loop waiting for you to tap the Final NMI test point to ground, to select test #1. After doing this, wait for 5 seconds before looking at the MO (to the right of the NMI T.P.) waveform in test 1. These tests are consecutive.

FINAL COMPUTER (Z-8002) DIAGNOSTICS	
F1	MO TOGGLE (see page 3.19)
F2	COMMON RAM (see page 3.20)
F3	DAC (see page 4/5.34)
F4-17	BIT TESTS (see page 4/5.35)

7. Test 17 wraps around to test 1. To resume normal operation:

   a. Switch power off.

   b. Remove Final NMI grounding jumper.

   c. Remove Main BREQ ground from Z-80.

   d. If necessary, replace DT8_4 with standard Main operating ROM.

   e. Switch power on.

   f. If necessary, reload programs (and sequences) through the cassette interface.

   g. To initialize Scratchpad, select both any Left and Right program.

F3 DAC TEST

As this test procedure produces loud "blurts" in the audio, turn down volume of the monitor system.

This test verifies the interrupt system, FIFO, and DAC.

For test setup instructions, see page 4/5.33.

1. Move scope probe to TP401 VDAC test point (located on PCB 4, between the DAC IC and TB402). You should observe this ascending linear ramp:

Figure 4/5.4.1.1
DAC TEST (GOOD)
V: 2V/div
H: .15 ms/div

2. Any hardware problems will probably appear as a non-linearity, such as in Figure 4/5.4.1.2, where a failure in one DAC bit is simulated:

Figure 4/5.4.1.2
DAC TEST (BAD)
D12 shorted

3. Problems with low-order bits may not be visible. For these, use the remaining bit tests.

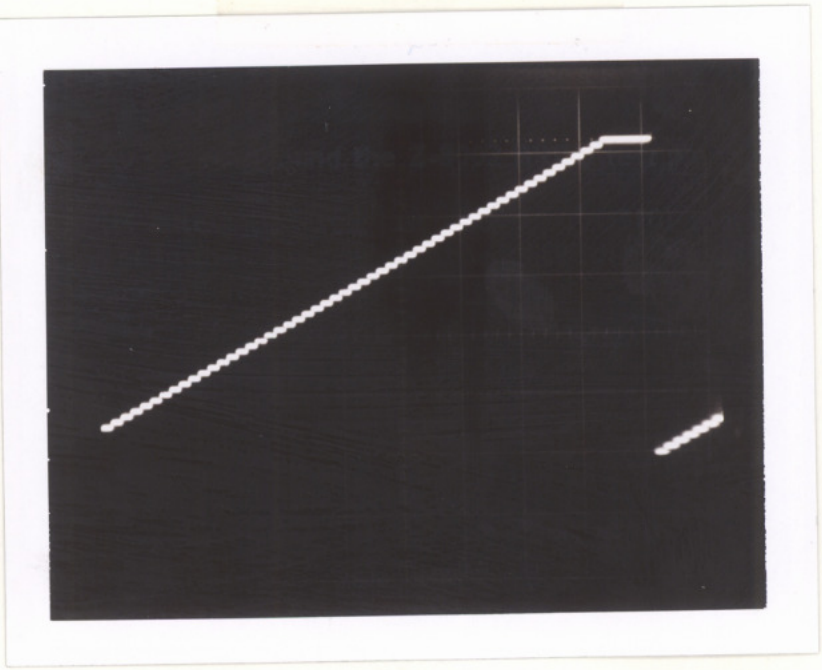


Figure 4/5.4.1.1

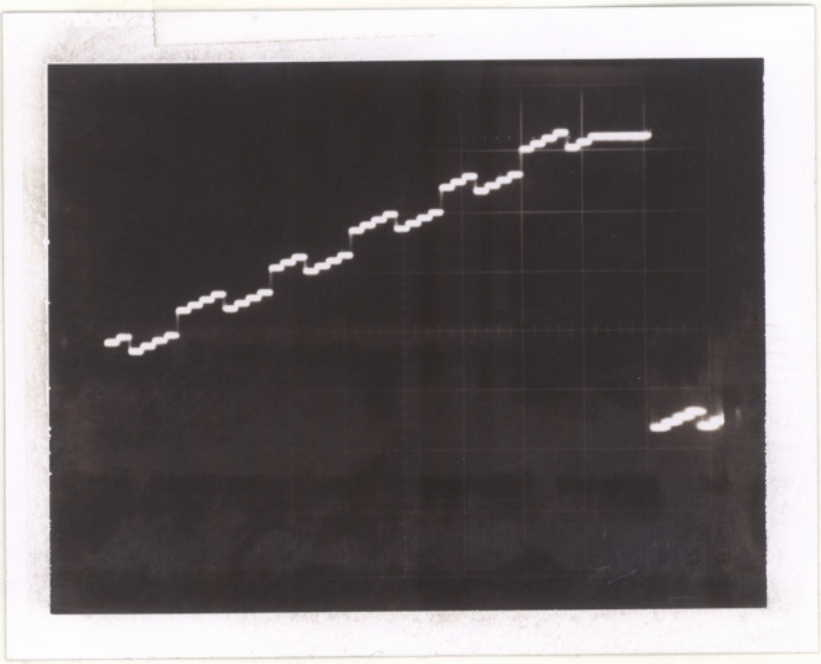


Figure 4/5.4.1.2

F4-17 BIT TESTS

This test exercises the low-order DAC bits, demultiplexer hardware, and sample/holds.

For test setup instructions, see page 4/5.33.

1. From this point on, each -NMI ground tap will set the next least-significant (LS) DAC bit and output this voltage to all sample/holds.

2. The DAC has a 10.666-V range. Each reading will be one half the value of the previous reading starting at 5.333 V (in theory). Theoretical voltage readings for each bit are shown in the following table. Keep in mind that offset variations will adjust each of these figures by +/- 0.010V.

High-Order Bits		Low-Order Bits	
Bit	V (typical)	Bit	V (typical)
0	+5.333	7	+0.041
1	+2.666	8	+0.021
2	+1.333	9	+0.010
3	+0.666	10	+0.005
4	+0.333	11	+0.0026
5	+0.166	12	-0.0013
6	+0.083	13	-0.0007

It may be difficult to read the values of bits 11-13 accurately. In most cases the computer will compensate for minor offsets, assuming all DAC bits are working, so this test is best-suited for checking the DAC circuit's basic operation.

(see next page)

3. When observed with a scope, each sample/hold should have a pure dc voltage, with a small amount of noise:

Figure 4/5.4.2.1
SAMPLE/HOLD (GOOD)

V: 10mV/div
H: .2us/div

4. After the last bit test, grounding -NMI again will recall Z-8002 test #1.

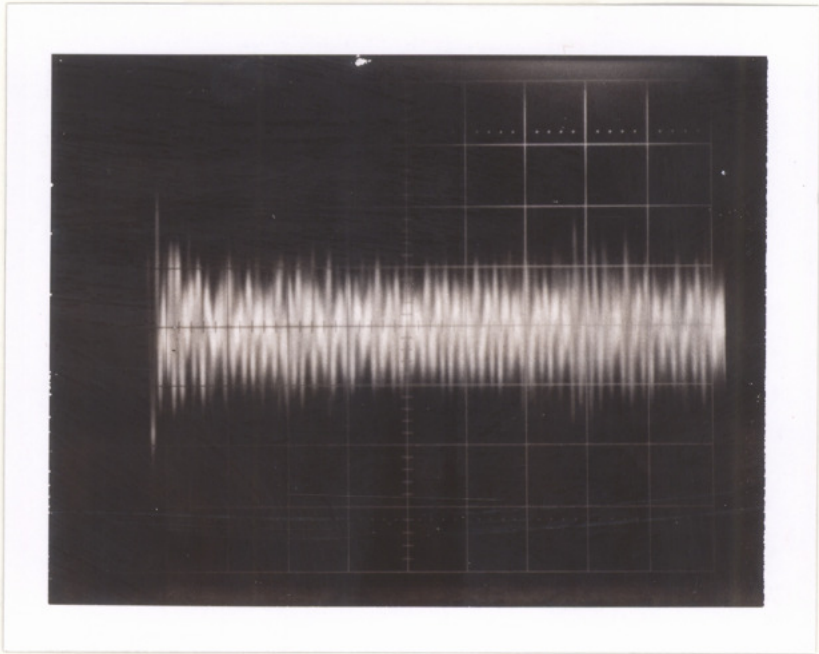


Figure 4/5.4.2.1

4/5.5 PCB 4 AND 5 VOICE BOARD REMOVAL

1. Raise boards (see page O.21).

2. If PCBs 4 and 5 have to be separated, desolder on PCB 5, as this will conform to the way the finished boards are stocked.

3. If PCB 4 has been replaced, be sure to apply a cable tie to the power cable (which runs from TB401 to P1504).

4/5.6 PCB 4 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
	Left Voice Board	Z-273L	PCB 4 Assembled
	Voice Power Cable	Z-283	PCB 4 Wiring Subassy

4/5.6.1 INTEGRATED CIRCUITS

Note: Only Voice 1 is described. Voices 2 through 8 are identical.

U401 OSC 1A I-321 CEM3340 VCO

The data sheet for the CEM3340 is at the back of this section. On the SUM input, R424 connects from the oscillator's frequency sample/hold, R425 sets the basic range of operation, and R426/C404 compensate the 3340's internal precision multiplier. U404-3 applies the OSC B P-MOD FREQ A CV. R404 adjusts OSC 1A scale by determining the current gain of the precision multiplier (along with R401 and R402) through the TEMPCO circuitry. Pull-down R403 helps with stability. R427 (pin 14) converts the current output of the precision multiplier into a drive voltage for the exponential current generator. R428 (pin 13) sets the reference current for the exponential generator. R429/C405 compensate the generator. C406 (pin 11) is the timing capacitor which is the main determinant of oscillator frequency range. It is a polystyrene type for low leakage and best stability. The PW MOD input is summed externally.

Notice that there is no analog switch on the pulse output, pin 4. To turn the pulse off the computer simply drives the pulse width all the way to dc. Because of interaction with the sync circuit, the computer must use +5V to disable the OSC A pulse.

When the SYNC CV goes to -5V, it enables Q401 to couple the falling edge of OSC B's sawtooth through C411 and R435. The internal comparator connected to U401-10 is thus pulled down to -5V, resetting the waveform. This hard-syncs OSC A to B. By clamping Q401's base to +5V, D404 ensures that when SYNC is off, negative pulses do not reach U401-10. SYNC CV is provided by converting the 0-5V SYNC latch signal to the required levels (+/-5V) on PCB 5 (see U506-4,-15).

U402-1 OSC 1A PW Summer I-312 TL082 DUAL BIFET OP AMP

This BIFET adds the Oscillator A PW CV from the sample/hold (through R407), -5V through R409 which sets initial range, and OSC B POLY-MOD output from U403-1. R408 sets a 10% amplification of the PW inputs. D401 limits the output voltage, because excessive voltage on the PW pin will shift the oscillator frequency.

U402-7 OSC 1A Wave Summer I-312 TL082 DUAL BIFET OP AMP

Any enabled waves are summed by U402-7 and ac-coupled to the Voice Processor (Filter) input.

U403-1 POLY-MOD PW Switch I-206 4016 QUAD ANALOG SWITCH

When on, connects OSC 1B output to Pulse Width Summer.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U403-3	OSC 1B Sawtooth Switch	I-206	4016 QUAD ANALOG SWITCH

When on, connects OSC 1B sawtooth output to OSC B Wave Summer.

U403-9	OSC 1A Triangle Switch	I-206	4016 QUAD ANALOG SWITCH

When on, connects OSC 1A triangle output to OSC 1A Wave Summer.

U403-10	OSC 1A Sawtooth Switch	I-206	4016 QUAD ANALOG SWITCH

When on, connects OSC 1A sawtooth output to OSC 1A Wave Summer.

U404-3	Poly-Mod Freq A Sw	I-243	4053 TRIPLE 1-OF-2 SWITCH

When on, applies OSC B Poly-Mod signal to OSC 1A frequency input.

U404-14	Osc 1B Triangle Switch	I-243	4053 TRIPLE 1-OF-2 SWITCH

When on, applies OSC 1B triangle output to Osc 1B Wave Summer. When off, R437 sums +5V to offset the +5V summed through R438 at Poly-Mod OSC B VCA.

U404-15	Poly-Mod Filter Sw	I-243	4053 TRIPLE 1-OF-2 SWITCH

When on, applies OSC B Poly-Mod signal to Filter frequency CV input of U407. When off, the input is grounded.

U405-1	OSC 1B Summers	I-312	TL082 DUAL BIFET OP AMP

Sums any enabled waves from OSC 1B. Drives both the Filter B input and the P-MOD OSC B VCA (U408-6).

U405-7	P-MOD VCA Buffer	I-312	TL082 DUAL BIFET OP AMP

Buffers P-MOD VCA output to the three P-MOD switches and destinations.

U406	OSC 1B	I-321	CEM3340 VCO

Similar to U401. The SUM input has a LO FREQ input. The pulse disable voltage is 0V so that no dc offset is created at pin 4 for either POLY-MOD destination when the pulse waveform is off.

U407	Voice 1 Processor	I-331	CEM3372 SIGNAL PROCESSOR

The Data Sheet for the CEM3372 is at the back of this section. Signal inputs are the summed A and B oscillator outputs. R422/23 set input impedance. A third input is from the Left Noise VCA, through C425 to pin -4 (CAP 1). The oscillator levels are controlled by the MIX A and B CVs. The noise level is controlled at its source by the noise VCA.

The filters are scaled at 1/2V/octave, to enable the various filter control sources--keyboard, LFO, ENV AMOUNT, CUTOFF to have full range. Filter frequency CV input is treated as a summing node. R455 FILTER 1 SCALE trims the input dividing resistors. R453 sets the basic filter range.

The main Filter CV comes from U435-8. The network D431/32, R4239/240 and C4144 provide local filtering for digitization noise (which is caused by the finite, 3-ms resolution of the envelopes). The filter basically offers two different slew rates, depending on the level

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION

U407 (continued) — Voice 1 Processor — I-331 — CEM3372 SIGNAL PROCESSOR

of the change. The Zener diodes are rated at 2.4V. When the filter envelope is moving slowly, the difference between the S/H output and the charge on C4144 will rarely exceed 2.4V. The diodes do not conduct, so the CV is slewed by R4239/C4144. When the difference exceeds 2.4V, one of the diodes switches on R4240 in parallel, which considerably accelerates the slewing. The diode which conducts depends on the direction of the CV difference. This two-speed filtering allows enough static filtering for acceptable noise without excessively distorting shorter envelopes.

CAPS 1 through 4 (C426-29) determine the frequency of each filter pole. The output from the fourth pole (pin 17) is ac-coupled to both a resonance VCA (pin 11) and the final VCA (pin 12). Divider R448/R450 determines the resonance point of the filter. In early versions these resistors were either 100K/3.6K or 27K/1K. These may have to be changed to the values 24K/1K if a Processor chip is replaced with a newer date code. Otherwise the voices may not break into Resonance at the same setting. Pin 10 is the RESONANCE CV input. The FILT RES CV drives all Left or Right 3372s in parallel.

The AMP CV receives digitization filtering similar to that for the Filter CV. But in this case, the high-speed slewing is switched in for a difference of .6V (rather than 2.4V).

The voice audio output is summed with the other three voices on that side.

Finally, note there is an interesting way the 3372 can fail which makes a simple situation look like a major calamity. All the MIX A and B CVs are common. Therefore if one of these inputs shorts internally to ground, all the OSC As or Bs (or both) will be disabled. To isolate the bad 3372 in this case you would probably measure the CV while alternately removing and reinstalling 3372s. (When the CV rises to normal you've found the bad IC.)

U408-2 — P-MOD OSC B VCA — I-327 — CEM3360 DUAL VCA

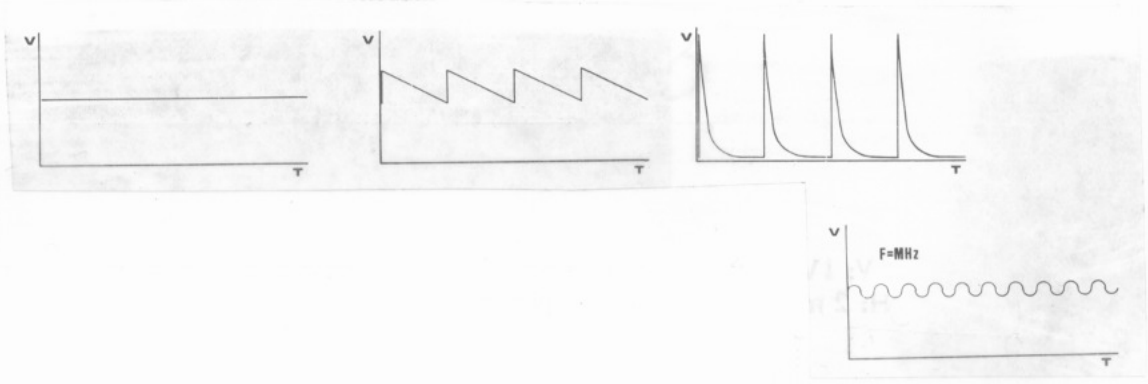
The Data Sheet for the CEM3360 is at the end of this section. The OSC 1B POLY-MOD level is controlled by VCA U408-2, buffered, and switched to OSC A FREQ by U404-3, to OSC A PW by U403-1, or to the filter by U404-15.

U408-13 — POLY-MOD OSC B VCA for Voice 2 — I-327 — CEM 3360 DUAL VCA

U409	OSC 2A	I-321	CEM3340 VCO
U410	Summers	I-312	TL082 DUAL BIFET OP AMP
U411	Switches	I-206	4016 QUAD ANALOG SWITCH
U412	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U413	Summers	I-312	TL082 DUAL BIFET OP AMP
U414	OSC 2B	I-321	CEM3340 VCO
U415	FILTER 2	I-331	CEM3372 SIGNAL PROCESSOR
U416	OSC 3A	I-321	CEM3340 VCO

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U417	Summers	I-312	TL082 DUAL BIFET OP AMP
U418	Switches	I-206	4016 QUAD ANALOG SWITCH
U419	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U420	Summers	I-312	TL082 DUAL BIFET OP AMP
U421	OSC 3B	I-321	CEM3340 VCO
U422	FILTER 3	I-331	CEM3372 SIGNAL PROCESSOR
U423	POLY-MOD OSC B VCA for Voices 3 and 4	I-327	CEM3360 DUAL VCA
U424	OSC 4A	I-321	CEM3340 VCO
U425	Summers	I-312	TL082 DUAL BIFET OP AMP
U426	Switches	I-206	4016 QUAD ANALOG SWITCH
U427	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U428	Summers	I-312	TL082 DUAL BIFET OP AMP
U429	OSC 4B	I-321	CEM3340 VCO
U430	FILTER 4	I-331	CEM3372 SIGNAL PROCESSOR
U431-34	Sample/Holds	I-332	TL084 (074) QUAD OP AMP

Below illustrates the output waveform of a typical S/H. Pure dc is desired. The output from a typical S/H should basically not "droop" during the interrupt cycle. When troubleshooting the synthesizer for malfunctions affecting all voices, it is a often a good idea to start by checking appropriate monophonic S/Hs.



GOOD **BAD** **BAD** **BAD**

Figure 4/5.6.1.1
SAMPLE/HOLD WAVEFORMS

Note that for all voices, the S/H for OSC B PW has some added resistors. The arrangement biases-down and expands the CV range to have complete control over the PW range.

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U435	Filter CV Filter for Voices 1-4 (see U407).	I-332	TL084 (074) QUAD OP AMP
U436-39	Demultiplexer	I-211	4051 8 TO 1 MUX
	One of eight outputs on each 4051 is selected with lines ABC. This number selects the destination S/H for each Vdac value, in combination with the I (inhibit) lines. EN0 through EN7 from U452/53 go low to selectively enable one active DMUX chip.		
U440-43	Sample/Holds See U431-34.	I-332	TL084 (074) QUAD OP AMP
U444	DAC Supply	I-403	78L05 +5V REGULATOR
	Derives a +5V analog supply for the DAC (pin -18).		
U445	DAC Buffer	I-323	LF356 FET OP AMP
	Converts the DAC output current to voltage, Vdac, which is distributed by the Demultiplexers on PCBs 4 and 5. Figure 4/5.6.1.2 shows a typical VDAC signal.		

V: 2V/div
H: .2 ms/div

Figure 4/5.6.1.2
VDAC, FACTORY PROGRAM "VIBALIMBA"

U446	DAC	I-502	DAC71-CSB-I 16-BIT DAC
	The DAC has a basic range from 0 to 10.666V. No trimmer is required.		

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U447-49	DAC Input Drivers	I-209	4049 HEX INVERTER
	The fourteen bits from the FIFO cross over from PCB 3. They are buffered and inverted to the active-low inputs which the DAC requires.		
U450	Address Counter	I-261	74HC393 Counter
	When clocked by the 62.5 kHz clock, creates the sample/hold addresses. The SHIFT signal (pin 4) goes to the FIFO Scan Logic. The most significant bits drive the Sample/Hold Decoder (U451). The next most significant bits are the ABC (1 of 8) addresses.		
U451	Sample/Hold Decoder	I-253	74HC138
	Disabled when S/H clear is high. When SHIFT is high, the ABC inputs decode one of the outputs -Y0-7 (active low).		
U452/53	Level Shifters	I-237	14504 HEX LEVEL SHIFTER
	U452 and 453 translate the +5-V address and enable strobes to +15V to control the +15V-operated 4051s.		
U454	Left Voice Summer	I-317	NE5534 LOW-NOISE OP AMP
	Combines the audio output from Voices 1-4.		

DESIGNATOR FUNCTION	SCI PART #	PART DESCRIPTION
4/5.6.2	**OTHER PARTS**	
C401/02	C-045	.1 50V 20% MONO RADIAL
C403-05	C-012	.01 50V 10% MYLAR RADIAL
C406	C-039	1000 pF 50V 5% POLY AXIAL
C407-10	C-045	.1 50V 20% MONO RADIAL
C411	C-005	220 pF 50V 10% DISC RADIAL
C412	C-045	.1 50V 20% MONO RADIAL
C413	C-046	.0056 100V MYLAR RADIAL
C414	C-045	.1 50V 20% MONO RADIAL
C415/16	C-012	.01 50V 10% MYLAR RADIAL
C417	C-039	1000 pF 50V 5% POLY AXIAL
C418-20	C-045	.1 50V 20% MONO RADIAL
C421/22	C-081	2.2 50V ELECT LOW LEAK
C423/24	C-064	2.2 50V NONPOLAR ELECT
C425	C-005	220 pF 50V 10% DISC RADIAL
C426	C-066	330 pF 50V 10% DISC AXIAL
C427-29	C-079	.033 10% MYLAR RADIAL
C430-32	C-045	.1 50V 20% MONO RADIAL
C433/34	C-012	.01 50V 10% MYLAR RADIAL
C435	C-039	1000 pF 50V 5% POLY AXIAL
C436	C-045	.1 50V 20% MONO RADIAL
C437	C-012	.01 50V 10% MYLAR RADIAL
C438-40	C-045	.1 50V 20% MONO RADIAL
C441	C-005	220 pF 50V 10% DISC RADIAL
C442	C-045	.1 50V 20% MONO RADIAL
C443/44	C-012	.01 50V 10% MYLAR RADIAL
C445	C-039	1000 pF 50V 5% POLY AXIAL
C446/47	C-045	.1 50V 20% MONO RADIAL
C448	C-005	220 pF 50V 10% DISC RADIAL
C449/50	C-045	.1 50V 20% MONO RADIAL
C451/52	C-064	2.2 50V NONPOLAR ELECT
C453	C-066	330 pF 50V 10% DISC AXIAL
C454-56	C-079	.033 10% MYLAR RADIAL
C457/58	C-081	2.2 50V ELECT LOW LEAK
C459-61	C-045	.1 50V 20% MONO RADIAL
C462/63	C-012	.01 50V 10% MYLAR RADIAL
C464	C-039	1000 pF 50V 5% POLY AXIAL
C465	C-045	.1 50V 20% MONO RADIAL
C466	C-012	.01 50V 10% MYLAR RADIAL
C467-69	C-045	.1 50V 20% MONO RADIAL
C470	C-005	220 pF 50V 10% DISC RADIAL
C471	C-045	.1 50V 20% MONO RADIAL
C472	C-046	.0056 100V MYLAR RADIAL
C473	C-045	.1 50V 20% MONO RADIAL
C474/75	C-012	.01 50V 10% MYLAR RADIAL
C476	C-039	1000 pF 50V 5% POLY AXIAL
C477/78	C-045	.1 50V 20% MONO RADIAL
C479	C-005	220 pF 50V 10% DISC RADIAL
C480/81	C-045	.1 50V 20% MONO RADIAL
C482/83	C-064	2.2 50V NONPOLAR ELECT
C484	C-066	330 pF 50V 10% DISC AXIAL

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
C485-87		C-079	.033 10% MYLAR RADIAL
C488/89		C-081	2.2 50V ELECT LOW LEAK
C490-92		C-045	.1 50V 20% MONO RADIAL
C493/94		C-012	.01 50V 10% MYLAR RADIAL
C495		C-039	1000 pF 50V 5% POLY AXIAL
C496		C-045	.1 50V 20% MONO RADIAL
C497		C-012	.01 50V 10% MYLAR RADIAL
C498-100		C-045	.1 50V 20% MONO RADIAL
C4101		C-005	220 pF 50V 10% DISC RADIAL
C4102		C-045	.1 50V 20% MONO RADIAL
C4103/104		C-012	.01 50V 10% MYLAR RADIAL
C4105		C-039	1000 pF 50V 5% POLY AXIAL
C4106/107		C-045	.1 50V 20% MONO RADIAL
C4108		C-005	220 pF 50V 10% DISC RADIAL
C4109		C-066	330 pF 50V 10% DISC AXIAL
C4110-112		C-079	.033 10% MYLAR RADIAL
C4113/114		C-064	2.2 50V NONPOLAR ELECT
C4115/116		C-045	.1 50V 20% MONO RADIAL
C4117/118		C-081	2.2 50V ELECT LOW LEAK
C4119		C-045	.1 50V 20% MONO RADIAL
C4120		C-012	.01 50V 10% MYLAR RADIAL
C4121		C-045	.1 50V 20% MONO RADIAL
C4122-125		C-012	.01 50V 10% MYLAR RADIAL
C4126		C-045	.1 50V 20% MONO RADIAL
C4127-130		C-012	.01 50V 10% MYLAR RADIAL
C4131		C-045	.1 50V 20% MONO RADIAL
C4132-135		C-012	.01 50V 10% MYLAR RADIAL
C4136		C-045	.1 50V 20% MONO RADIAL
C4137-140		C-012	.01 50V 10% MYLAR RADIAL
C4141-145		C-045	.1 50V 20% MONO RADIAL
C4146		C-003	33 pF 50V 10% DISC RADIAL
C4147		C-045	.1 50V 20% MONO RADIAL
C4148-155		C-012	.01 50V 10% MYLAR RADIAL
C4156		C-045	.1 50V 20% MONO RADIAL
C4157-160		C-012	.01 50V 10% MYLAR RADIAL
C4161		C-045	.1 50V 20% MONO RADIAL
C4162-166		C-012	.01 50V 10% MYLAR RADIAL
C4167		C-054	10 35V ELECT TANT
C4168		C-020	1.0 25V 20% TANT RADIAL
C4169		C-047	120 pF 10% DISC RADIAL
C4170		C-012	.01 50V 10% MYLAR RADIAL
C4171-173		C-020	1.0 25V 20% TANT RADIAL
C4174-176		C-045	.1 50V 20% MONO RADIAL
C4177		C-020	1.0 25V 20% TANT RADIAL
C4178/79		C-045	.1 50V 20% MONO RADIAL
C4180		C-012	.01 50V 10% MYLAR RADIAL
C4181		C-045	.1 50V 20% MONO RADIAL
C4182		C-012	.01 50V 10% MYLAR RADIAL
C4183		C-045	.1 50V 20% MONO RADIAL
C4184		C-003	33 pF 50V 10% DISC RADIAL

(C4184 was "kludged" in early versions.)

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
D401-03		D-005	1N914
D404		D-008	1N34
D405-08		D-005	1N914
D409		D-008	1N34
D410-14		D-005	1N914
D415		D-008	1N34
D416-19		D-005	1N914
D420		D-008	1N34
D421-24		D-009	1N5221 2.4V ZENER
D425-28		D-005	1N914
D429-32		D-009	1N5221 2.4V ZENER
D433-36		D-005	1N914
J401	See TB401	J-047	9-PIN JACK
P401		P-076	40-PIN HEADER
Q401-04		T-003	2N4250
R401		R-191	6.04K, 1%
R402		R-146	26.7K, 1%
R403		R-192	1.50M, 1%
R404	OSC 1A SCALE	R-211	5K TRIMMER TOP ADJ
R405		R-015	20K
R406		R-029	1M
R407		R-110	100K, 1%
R408		R-159	110K, 1%
R409		R-110	100K, 1%
R410		R-029	1M
R411		R-110	100K, 1%
R412		R-122	200K, 1%
R413		R-188	332K, 1%
R414		R-029	1M
R415		R-015	20K
R416		R-191	6.04K, 1%
R417		R-146	26.7K, 1%
R418		R-192	1.50M, 1%
R419	OSC 1B SCALE	R-211	5K TRIMMER TOP ADJ
R420		R-012	10K
R421		R-018	47K
R422/23		R-008	1K
R424		R-110	100K, 1%
R425		R-408	294K, 1%
R426		R-006	470
R427		R-139	182K, 1%
R428		R-116	2.21M, 1%
R429		R-006	470
R430		R-028	470K
R431		R-027	390K
R432		R-029	1M
R433		R-028	470K
R434		R-018	47K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R435		R-012	10K
R436/37		R-160	499K, 1%
R438		R-115	301K, 1%
R439		R-110	100K, 1%
R440		R-148	49.9K, 1%
R441/42		R-110	100K, 1%
R443		R-408	294K, 1%
R444		R-006	470
R445		R-139	1.82K, 1%
R446		R-006	470
R447		R-116	2.21M, 1%
R448-49		R-073	24K
R450		R-008	1K
R451		R-146	26.7K, 1%
R452/53		R-110	100K, 1%
R454		R-139	1.82K, 1%
R455	FILTER 1 SCALE	R-209	1K TRIMMER TOP ADJ
R456		R-191	6.04K, 1%
R457		R-146	26.7K, 1%
R458		R-192	1.50M, 1%
R459	OSC 2A SCALE	R-211	5K TRIMMER TOP ADJ
R460		R-015	20K
R461		R-029	1M
R462		R-110	100K, 1%
R463		R-159	110K, 1%
R464		R-110	100K, 1%
R465		R-029	1M
R466		R-110	100K, 1%
R467		R-122	200K, 1%
R468		R-110	100K, 1%
R469		R-115	301K, 1%
R470		R-188	332K, 1%
R471		R-029	1M
R472		R-015	20K
R473		R-191	6.04K, 1%
R474		R-146	26.7K, 1%
R475		R-192	1.50M, 1%
R476		R-021	68K
R477	OSC 2B SCALE	R-211	5K TRIMMER TOP ADJ
R478		R-012	10K
R479		R-018	47K
R480/81		R-008	1K
R482		R-110	100K, 1%
R483		R-408	294K, 1%
R484		R-006	470
R485		R-139	1.82K, 1%
R486		R-116	2.21M, 1%
R487		R-006	470
R488		R-028	470K
R489		R-027	390K
R490		R-029	1M
R491		R-028	470K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R492		R-018	47K
R493		R-012	10K
R494/95		R-160	499K, 1%
R496		R-148	49.9K, 1%
R497/98		R-110	100K, 1%
R499		R-408	294K, 1%
R4100		R-006	470
R4101		R-139	1.82K, 1%
R4102		R-006	470
R4103		R-116	2.21M, 1%
R4104/105		R-073	24K
R4106		R-008	1K
R4107		R-146	26.7K, 1%
R4108	FILTER 2 SCALE	R-209	1K TRIMMER TOP ADJ
R4109/110		R-110	100K, 1%
R4111		R-139	1.82K, 1%
R4112		R-191	6.04K, 1%
R4113		R-146	26.7K, 1%
R4114		R-192	1.50M, 1%
R4115	OSC 3A SCALE	R-211	5K TRIMMER TOP ADJ
R4116		R-015	20K
R4117		R-029	1M
R4118		R-110	100K, 1%
R4119		R-159	110K, 1%
R4120		R-110	100K, 1%
R4121		R-029	1M
R4122		R-110	100K, 1%
R4123		R-122	200K, 1%
R4124		R-188	332K, 1%
R4125		R-029	1M
R4126		R-015	20K
R4127		R-191	6.04K, 1%
R4128		R-146	26.7K, 1%
R4129		R-192	1.50M, 1%
R4130	OSC 3B SCALE	R-211	5K TRIMMER TOP ADJ
R4131		R-021	68K
R4132		R-012	10K
R4133		R-018	47K
R4134/135		R-008	1K
R4136		R-110	100K, 1%
R4137		R-408	294K, 1%
R4138		R-006	470
R4139		R-139	1.82K, 1%
R4140		R-116	2.21M, 1%
R4141		R-006	470
R4142		R-028	470K
R4143		R-027	390K
R4144		R-029	1M
R4145		R-028	470K
R4146		R-012	10K
R4147		R-018	47K
R4148/149		R-160	499K, 1%

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R4150		R-115	301K, 1%
R4151		R-110	100K, 1%
R4152		R-148	49.9K, 1%
R4153/154		R-110	100K, 1%
R4155		R-408	294K, 1%
R4156		R-006	470
R4157		R-139	1.82K, 1%
R4158		R-006	470
R4159		R-116	2.21M, 1%
R4160/161		R-073	24K
R4162		R-008	1K
R4163		R-146	26.7K, 1%
R4164	FILTER 3 SCALE	R-209	1K TRIMMER TOP ADJ
R4165/166		R-110	100K, 1%
R4167		R-139	1.82K, 1%
R4168		R-191	6.04K, 1%
R4169		R-146	26.7K, 1%
R4170		R-192	1.50M, 1%
R4171	OSC 4A SCALE	R-211	5K TRIMMER TOP ADJ
R4172		R-015	20K
R4173		R-029	1M
R4174		R-110	100K, 1%
R4175		R-159	110K, 1%
R4176		R-110	100K, 1%
R4177		R-029	1M
R4178		R-110	100K, 1%
R4179		R-122	200K, 1%
R4180		R-110	100K, 1%
R4181		R-115	301K, 1%
R4182		R-188	332K, 1%
R4183		R-029	1M
R4184		R-015	20K
R4185		R-191	6.04K, 1%
R4186		R-146	26.7K, 1%
R4187		R-192	1.50M, 1%
R4188		R-021	68K
R4189	OSC 4B SCALE	R-211	5K TRIMMER TOP ADJ
R4190		R-012	10K
R4191		R-018	47K
R4192/193		R-008	1K
R4194		R-110	100K, 1%
R4195		R-408	294K, 1%
R4196		R-006	470
R4197		R-139	1.82K, 1%
R4198		R-116	2.21M, 1%
R4199		R-006	470
R4200		R-028	470K
R4201		R-027	390K
R4202		R-029	1M
R4203		R-028	470K
R4204		R-012	10K
R4205		R-018	47K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R4206/207		R-160	499K, 1%
R4208		R-148	49.9K, 1%
R4209/210		R-110	100K, 1%
R4211		R-408	294K, 1%
R4212		R-006	470
R4213		R-139	1.82K, 1%
R4214		R-006	470
R4215		R-116	2.21M, 1%
R4216/217		R-073	24K
R4218		R-008	1K
R4219		R-146	26.7K, 1%
R4220	FILTER 4 SCALE	R-209	1K TRIMMER TOP ADJ
R4221/222		R-110	100K, 1%
R4223		R-139	1.82K, 1%
R4224		R-029	1M
R4225		R-012	10K
R4226		R-025	100K
R4227		R-029	1M
R4228		R-012	10K
R4229		R-025	100K
R4230		R-008	1K
R4231/232		R-018	47K
R4233		R-008	1K
R4234		R-025	100K
R4235		R-067	3.9K
R4236		R-047	10
R4237		R-008	1K
R4238/239		R-018	47K
R4240		R-008	1K
R4241		R-067	3.9K
R4242		R-025	100K
R4243		R-067	3.9K
R4244/245		R-025	100K
R4246		R-067	3.9K
R4247		R-017	39K
R4248		R-029	1M
R4249		R-012	10K
R4250/251		R-025	100K
R4252		R-029	1M
R4253		R-012	10K
R4254		R-142	5.62K, 1%
R4255		R-162	332, 1%
R4256		R-008	1K
R4257		R-021	68K
TB401		Z-283	Wiring Subassy
J401		J-047	9-PIN JACK
	Used with J401	P-028	GOLD SOCKET CONTACTS
TB402		E-147	10-PIN 1" JUMPER
TB403-05		E-148	11-PIN 1" JUMPER

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
TP401	Vdac		
		J-007	16-PIN DIP SOCKET
		J-017	24-PIN DIP SOCKET
		J-027	14-PIN DIP SOCKET
		J-041	18-PIN DIP SOCKET
		PC1008-4	PCB 4

Rev B required modifications in demultiplexer, resonance resistors, and audio summer capacitors.
Rev C has no modifications.

4/5.7 PCB 5 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
	Right Voice Board	Z-273R	PCB 5 Assembled
	Voice Audio Cable	Z-284	PCB 5 Wiring Subassy

4/5.7.1 INTEGRATED CIRCUITS

Note: For discussion of sample/holds and Synthesizer Voice, see pages 4/5.38-43.

U501-03	Sample/Holds See U431.	I-332	TL084 (074) QUAD OP AMP
U504	Filter CV Filter See U407.	I-312	TL082 DUAL BIFET OP AMP
U505	Tune Comparator Converts the analog wave from the Tune Multiplexer into the pulse which clocks the Tune Cycle Counter. This output will be grounded if TUNE EN is low.	I-301	LM311 PRECISION CPR
U506-14	Tune L/R Select Taps audio from either the Left or Right Voice Summers.	I-243	4053 TRIPLE 1-OF-2 SWITCH
U506-4, -15	L/R Sync CV When on, these select -5V, which enables all four sync circuits on one side.	I-243	4053 TRIPLE 1-OF-2 SWITCH
U507	Right Voice Summer Combines the audio outputs of Voices 5-8.	I-317	NE5534 LOW-NOISE OP AMP
U508	Miscellaneous Buffer See U514 or U515.	I-332	TL084 (074) QUAD OP AMP
U509	Left/Right Noise VCA Adjusts Noise level to Left and Right voices (buffered by U508).	I-327	CEM3360 DUAL VCA
U510-13	Demultiplexers	I-211	4051 8 TO 1 MUX
U514	L/R OSC B LO Switches The OSC B LO switches apply the stable 15V analog supply to an inverting amplifier (U508) and scaling resistors R526/18 and R527/19. This creates the negative bias used to push down OSC B's low frequency range (which is easier than asking the DAC to go negative!). D513/14 protect the input of the switch from climbing to +15V when the switch is off. In Rev B, U514-11 is "jumpered" to U508-13.	I-206	4016 QUAD ANALOG SWITCH
U515	White Noise Source Noise is ac-coupled (to reduce sub-sonics) to the Left and Right Noise VCAs, then buffered by U508. The Noise L returns to PCB 4. Noise R stays on PCB 5.	I-333	5437 DIGITAL NOISE SOURCE

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
U516-19	Sample/Holds	I-332	TL084 (074) QUAD OP AMP
	One half of U519 acts as a filter CV filter for voices 7 and 8.		
U520	OSC 5A	I-321	CEM3340 VCO
U521	Switches	I-206	4016 QUAD ANALOG SWITCH
U522	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U523	Summers	I-312	TL082 DUAL BIFET OP AMP
U524	OSC 5B	I-321	CEM3340 VCO
U525	Voice 5 Processer	I-331	CEM3372 SIGNAL PROCESSOR
U526	P-MOD OSC B VCA	I-327	CEM3360 DUAL VCA
U527	OSC 6A	I-321	CEM3340 VCO
U528	Summers	I-312	TL082 DUAL BIFET OP AMP
U529	Switches	I-206	4016 QUAD ANALOG SWITCH
U530	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U531	Summers	I-312	TL082 DUAL BIFET OP AMP
U532	OSC 6B	I-321	CEM3340 VCO
U533	Voice 6 Processor	I-331	CEM3372 SIGNAL PROCESSOR
U534	OSC 7A	I-321	CEM3340 VCO
U535	Summers	I-312	TL082 DUAL BIFET OP AMP
U536	Switches	I-206	4016 QUAD ANALOG SWITCH
U537	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U538	Summers	I-312	TL082 DUAL BIFET OP AMP
U539	OSC 7B	I-321	CEM3340 VCO
U540	Voice 7 Processor	I-331	CEM3372 SIGNAL PROCESSOR
U541	P-MOD OSC B VCA	I-327	CEM3360 DUAL VCA
U542	OSC 8A	I-321	CEM3340 VCO
U543	Summers	I-312	TL082 DUAL BIFET OP AMP
U544	Switches	I-206	4016 QUAD ANALOG SWITCH
U545	Switches	I-243	4053 TRIPLE 1-OF-2 SWITCH
U546	Summers	I-312	TL082 DUAL BIFET OP AMP
U547	OSC 8B	I-321	CEM3340 VCO
U548	Voice 8 Processor	I-331	CEM3372 SIGNAL PROCESSOR
U549	Summers	I-312	TL082 DUAL BIFET OP AMP

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
4/5.7.2		**OTHER PARTS**	
C501		C-012	.01 50V 10% MYLAR RADIAL
C502		C-045	.1 50V 20% MONO RADIAL
C503-06		C-012	.01 50V 10% MYLAR RADIAL
C507		C-045	.1 50V 20% MONO RADIAL
C508-12		C-012	.01 50V 10% MYLAR RADIAL
C513		C-045	.1 50V 20% MONO RADIAL
C514-17		C-012	.01 50V 10% MYLAR RADIAL
C518-24		C-045	.1 50V 20% MONO RADIAL
C525		C-005	220 pF 50V 10% DISC RADIAL
C526/27		C-045	.1 50V 20% MONO RADIAL
C528		C-003	33 pF 50V 10% DISC RADIAL
C529		C-045	.1 50V 20% MONO RADIAL
C530		C-046	.0056 100V MYLAR RADIAL
C531		C-005	220 pF 50V 10% DISC RADIAL
C532		C-021	2.2 25V 20% TANT RADIAL
C533/34		C-045	.1 50V 20% MONO RADIAL
C535-38		C-012	.01 50V 10% MYLAR RADIAL
C539		C-045	.1 50V 20% MONO RADIAL
C540-43		C-012	.01 50V 10% MYLAR RADIAL
C544		C-045	.1 50V 20% MONO RADIAL
C545-49		C-012	.01 50V 10% MYLAR RADIAL
C550		C-045	.1 50V 20% MONO RADIAL
C551/52		C-012	.01 50V 10% MYLAR RADIAL
C553/54		C-045	.1 50V 20% MONO RADIAL
C555		C-012	.01 50V 10% MYLAR RADIAL
C556/57		C-045	.1 50V 20% MONO RADIAL
C558		C-012	.01 50V 10% MYLAR RADIAL
C559/60		C-045	.1 50V 20% MONO RADIAL
C561		C-005	220 pF 50V 10% DISC RADIAL
C562		C-066	330 pF 50V 10% DISC AXIAL
C563		C-064	2.2 50V NONPOLAR ELECT
C564		C-079	.033 10% MYLAR RADIAL
C565		C-064	2.2 50V NONPOLAR ELECT
C566/67		C-079	.033 10% MYLAR RADIAL
C568-70		C-045	.1 50V 20% MONO RADIAL
C571/72		C-081	2.2 50V ELECT LOW LEAK
C573		C-045	.1 50V 20% MONO RADIAL
C574/75		C-012	.01 50V 10% MYLAR RADIAL
C576		C-039	1000 pF 50V 5% POLY AXIAL
C577-80		C-045	.1 50V 20% MONO RADIAL
C581		C-005	220 pF 50V 10% DISC RADIAL
C582		C-045	.1 50V 20% MONO RADIAL
C583		C-046	.0056 100V MYLAR RADIAL
C584/85		C-012	.01 50V 10% MYLAR RADIAL
C586		C-039	1000 pF 50V 5% POLY AXIAL
C587		C-012	.01 50V 10% MYLAR RADIAL
C588-91		C-045	.1 50V 20% MONO RADIAL
C592		C-005	220 pF 50V 10% DISC RADIAL
C593		C-066	330 pF 50V 10% DISC AXIAL
C594		C-064	2.2 50V NONPOLAR ELECT

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
C595		C-079	.033 10% MYLAR RADIAL
C596		C-064	2.2 50V NONPOLAR ELECT
C597/98		C-079	.033 10% MYLAR RADIAL
C599-101		C-045	.1 50V 20% MONO RADIAL
C5102/103		C-081	2.2 50V ELECT LOW LEAK
C5104		C-045	.1 50V 20% MONO RADIAL
C5105/106		C-012	.01 50V 10% MYLAR RADIAL
C5107		C-039	1000 pF 50V 5% POLY AXIAL
C5108-111		C-045	.1 50V 20% MONO RADIAL
C5112		C-005	220 pF 50V 10% DISC RADIAL
C5113/114		C-012	.01 50V 10% MYLAR RADIAL
C5115		C-039	1000 pF 50V 5% POLY AXIAL
C5116/117		C-045	.1 50V 20% MONO RADIAL
C5118		C-012	.01 50V 10% MYLAR RADIAL
C5119/120		C-045	.1 50V 20% MONO RADIAL
C5121		C-005	220 pF 50V 10% DISC RADIAL
C5122		C-066	330 pF 50V 10% DISC AXIAL
C5123		C-064	2.2 50V NONPOLAR ELECT
C5124		C-079	.033 10% MYLAR RADIAL
C5125		C-064	2.2 50V NONPOLAR ELECT
C5126/127		C-079	.033 10% MYLAR RADIAL
C5128-130		C-045	.1 50V 20% MONO RADIAL
C5131-132		C-081	2.2 50V ELECT LOW LEAK
C5133		C-045	.1 50V 20% MONO RADIAL
C5134/135		C-012	.01 50V 10% MYLAR RADIAL
C5136		C-039	1000 pF 50V 5% POLY AXIAL
C5137-140		C-045	.1 50V 20% MONO RADIAL
C5141		C-005	220 pF 50V 10% DISC RADIAL
C5142		C-045	.1 50V 20% MONO RADIAL
C5143		C-046	.0056 100V MYLAR RADIAL
C5144/145		C-012	.01 50V 10% MYLAR RADIAL
C5146		C-039	1000 pF 50V 5% POLY AXIAL
C5147-148		C-045	.1 50V 20% MONO RADIAL
C5149		C-012	.01 50V 10% MYLAR RADIAL
C5150-151		C-045	.1 50V 20% MONO RADIAL
C5152		C-005	220 pF 50V 10% DISC RADIAL
C5153		C-066	330 pF 50V 10% DISC AXIAL
C5154		C-064	2.2 50V NONPOLAR ELECT
C5155/156		C-079	.033 10% MYLAR RADIAL
C5157		C-064	2.2 50V NONPOLAR ELECT
C5158		C-079	.033 10% MYLAR RADIAL
C5159-161		C-045	.1 50V 20% MONO RADIAL
C5162/163		C-081	2.2 50V ELECT LOW LEAK
C5164/165		C-012	.01 50V 10% MYLAR RADIAL
C5166		C-039	1000 pF 50V 5% POLY AXIAL
C5167-170		C-045	.1 50V 20% MONO RADIAL
C5171		C-005	220 pF 50V 10% DISC RADIAL
C5172/173		C-012	.01 50V 10% MYLAR RADIAL
C5174		C-039	1000 pF 50V 5% POLY AXIAL
C5175		C-045	.1 50V 20% MONO RADIAL
C5176		C-003	33 pF 50V 10% DISC RADIAL

(C5176 "kludged" in early versions).

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
D501-04		D-005	1N914
D505-12		D-009	1N5221 2.4V ZENER
D513-22		D-005	1N914
D523		D-008	1N34
D524-527		D-005	1N914
D528		D-008	1N34
D529-32		D-005	1N914
D533		D-008	1N34
D534-37		D-005	1N914
D538		D-008	1N34
J501	See TB501.	J-084	7-PIN LOCKING HOUSING
	Used with J501	P-049	GOLD SOCKET CONTACTS
	Used at J501-6	P-031	POLARIZING PIN
Q501-04		T-003	2N4250
R501		R-029	1M
R502		R-012	10K
R503		R-025	100K
R504		R-012	10K
R505		R-025	100K
R506		R-029	1M
R507		R-025	100K
R508		R-067	3.9K
R509		R-025	100K
R510		R-067	3.9K
R511		R-008	1K
R512/13		R-018	47K
R514		R-008	1K
R515		R-029	1M
R516		R-011	4.7K
R517		R-025	100K
R518/19		R-414	64.9K, 1%
R520		R-068	100
R521/22		R-012	10K
R523		R-017	39K
	R523 must be insulated from the rail.		
R524/25		R-018	47K
R526/27		R-110	100K, 1%
R528/29		R-072	12K
R530		R-008	1K
R531		R-018	47K
R532		R-008	1K
R533		R-018	47K
R534		R-025	100K
R535		R-067	3.9K
R536		R-025	100K
R537		R-067	3.9K
R538		R-025	100K
R539		R-029	1M
R540		R-012	10K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R541		R-029	1M
R542		R-012	10K
R543		R-025	100K
R544		R-191	6.04K, 1%
R545		R-146	26.7K, 1%
R546		R-192	1.50M, 1%
R547	OSC 5A SCALE	R-211	5K TRIMMER TOP ADJ
R548		R-015	20K
R549		R-029	1M
R550		R-110	100K, 1%
R551		R-159	110K, 1%
R552		R-110	100K, 1%
R553		R-068	100
R554		R-029	1M
R555		R-110	100K, 1%
R556		R-122	200K, 1%
R557		R-188	332K, 1%
R558		R-029	1M
R559		R-015	20K
R560		R-191	6.04K, 1%
R561		R-146	26.7K, 1%
R562		R-192	1.50M, 1%
R563	OSC 5B SCALE	R-211	5K TRIMMER TOP ADJ
R564		R-012	10K
R565		R-018	47K
R566/67		R-008	1K
R568		R-110	100K, 1%
R569		R-408	294K, 1%
R570		R-006	470
R571		R-139	1.82K, 1%
R572		R-116	2.21M, 1%
R573		R-006	470
R574		R-028	470K
R575		R-027	390K
R576		R-029	1M
R577		R-028	470K
R578		R-018	47K
R579		R-012	10K
R580/81		R-160	499K, 1%
R582		R-115	301K, 1%
R583		R-110	100K, 1%
R584		R-148	49.9K, 1%
R585/86		R-110	100K, 1%
R587		R-408	294K, 1%
R588		R-006	470
R589		R-139	1.82K, 1%
R590		R-006	470
R591		R-116	2.21M, 1%
R592		R-191	6.04K, 1%
R593		R-146	26.7K, 1%
R594	FILTER 5 SCALE	R-209	1K TRIMMER TOP ADJ
R595/96		R-073	24K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R597/98		R-110	100K, 1%
R599		R-139	1.82K, 1%
R5100		R-021	68K
R5101		R-191	6.04K, 1%
R5102		R-146	26.7K, 1%
R5103		R-192	1.50M, 1%
R5104	OSC 6A SCALE	R-211	5K TRIMMER TOP ADJ
R5105		R-015	20K
R5106		R-029	1M
R5107		R-110	100K, 1%
R5108		R-159	110K, 1%
R5109		R-110	100K, 1%
R5110		R-029	1M
R5111		R-110	100K, 1%
R5112		R-122	200K, 1%
R5113		R-110	100K, 1%
R5114		R-115	301K, 1%
R5115		R-188	332K, 1%
R5116		R-029	1M
R5117		R-015	20K
R5118		R-191	6.04K, 1%
R5119		R-146	26.7K, 1%
R5120		R-192	1.50M, 1%
R5121	OSC 6B SCALE	R-211	5K TRIMMER TOP ADJ
R5122		R-012	10K
R5123		R-018	47K
R5124/125		R-008	1K
R5126		R-110	100K, 1%
R5127		R-408	294K, 1%
R5128		R-006	470
R5129		R-139	1.82K, 1%
R5130		R-116	2.21M, 1%
R5131		R-006	470
R5132		R-028	470K
R5133		R-027	390K
R5134		R-029	1M
R5135		R-028	470K
R5136		R-018	47K
R5137		R-012	10K
R5138/139		R-160	499K, 1%
R5140		R-148	49.9K, 1%
R5141/142		R-110	100K, 1%
R5143		R-408	294K, 1%
R5144		R-006	470
R5145		R-139	1.82K, 1%
R5146		R-006	470
R5147		R-116	2.21M, 1%
R5148		R-146	26.7K, 1%
R5149	FILTER 6 SCALE	R-209	1K TRIMMER TOP ADJ
R5150/151		R-073	24K
R5152		R-008	1K
R5153/154		R-110	100K, 1%

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R5155		R-139	1.82K, 1%
R5156		R-021	68K
R5157		R-146	26.7K, 1%
R5158		R-192	1.50M, 1%
R5159	OSC 7A SCALE	R-211	5K TRIMMER TOP ADJ
R5160		R-015	20K
R5161		R-029	1M
R5162		R-110	100K, 1%
R5163		R-159	110K, 1%
R5164		R-110	100K, 1%
R5165		R-029	1M
R5166		R-110	100K, 1%
R5167		R-122	200K, 1%
R5168		R-188	332K, 1%
R5169		R-029	1M
R5170		R-015	20K
R5171		R-191	6.04K, 1%
R5172		R-146	26.7K, 1%
R5173		R-192	1.50M, 1%
R5174	OSC 7B SCALE	R-211	5K TRIMMER TOP ADJ
R5175		R-012	10K
R5176		R-018	47K
R5177/178		R-008	1K
R5179		R-110	100K, 1%
R5180		R-408	294K, 1%
R5181		R-006	470
R5182		R-139	1.82K, 1%
R5183		R-116	2.21M, 1%
R5184		R-006	470
R5185		R-028	470K
R5186		R-027	390K
R5187		R-029	1M
R5188		R-028	470K
R5189		R-018	47K
R5190		R-012	10K
R5191/192		R-160	499K, 1%
R5193		R-115	301K, 1%
R4194		R-110	100K, 1%
R5195		R-148	49.9K, 1%
R5196/197		R-110	100K, 1%
R5198		R-408	294K, 1%
R5199		R-006	470
R5200		R-139	1.82K, 1%
R5201		R-006	470
R5202		R-116	2.21M, 1%
R5203		R-146	26.7K, 1%
R5204	FILTER 7	R-209	1K TRIMMER TOP ADJ
R5205/206		R-073	24K
R5207		R-008	1K
R5208/209		R-110	100K, 1%
R5210		R-139	1.82K, 1%
R5211		R-021	68K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
R5212		R-191	6.04K, 1%
R5213		R-146	26.7K, 1%
R5214		R-192	1.50M, 1%
R5215	OSC 8A SCALE	R-211	5K TRIMMER TOP ADJ
R5216		R-015	20K
R5217		R-029	1M
R5218		R-110	100K, 1%
R5219		R-159	110K, 1%
R5220		R-110	100K, 1%
R5221		R-029	1M
R5222		R-110	100K, 1%
R5223		R-122	200K, 1%
R5224		R-110	100K, 1%
R5225		R-115	301K, 1%
R5226		R-188	332K, 1%
R5227		R-029	1M
R5228		R-015	20K
R5229		R-191	6.04K, 1%
R5230		R-146	26.7K, 1%
R5231		R-192	1.50M, 1%
R5232	OSC 8B SCALE	R-211	5K TRIMMER TOP ADJ
R5233		R-012	10K
R5234		R-018	47K
R5235/236		R-008	1K
R5237		R-110	100K, 1%
R5238		R-408	294K, 1%
R5239		R-006	470
R5240		R-139	1.82K, 1%
R5241		R-116	2.21M, 1%
R5242		R-006	470
R5243		R-028	470K
R5244		R-027	390K
R5245		R-029	1M
R5246		R-028	470K
R5247		R-018	47K
R5248		R-012	10K
R5249/250		R-160	499K, 1%
R5251		R-148	49.9K, 1%
R5252/253		R-110	100K, 1%
R5254		R-408	294K, 1%
R5255		R-006	470
R5256		R-139	1.82K, 1%
R5257		R-006	470
R5258		R-116	2.21M, 1%
R5259		R-021	68K
R5260		R-146	26.7K, 1%
R5261	FILTER 8 SCALE	R-209	1K TRIMMER TOP ADJ
R5262/263		R-073	24K
R5264		R-008	1K
R5265/266		R-110	100K, 1%
R5267		R-139	1.82K, 1%
R5268		R-008	1K

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
TB501		Z-284	Wiring Subassy
		E-045	Thin coax
	Notice that coax is grounded to TB501, but not to J501.		
TB502-05	(See TB402-05)		
		J-007	16-PIN DIP SOCKET
		J-027	14-PIN DIP SOCKET
		J-041	18-PIN DIP SOCKET
		PC1008-5	PCB 5
	Rev B required jumper in OSC B LO, and added audio summer capacitor.		
	Rev C requires R523 be insulated from rail.		

4/5.8 DATA SHEETS

CEM3340
CEM3360
CEM3372

CEM 3340 / 3345

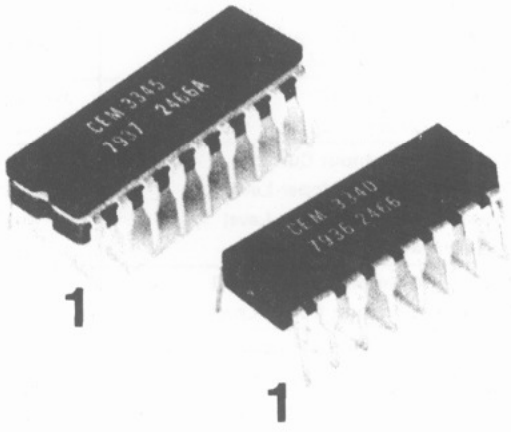
CURTIS ELECTROMUSIC SPECIALTIES
2900 Mauricia Ave.
Santa Clara, CA 95051
(408) 247-8046

Voltage Controlled Oscillator

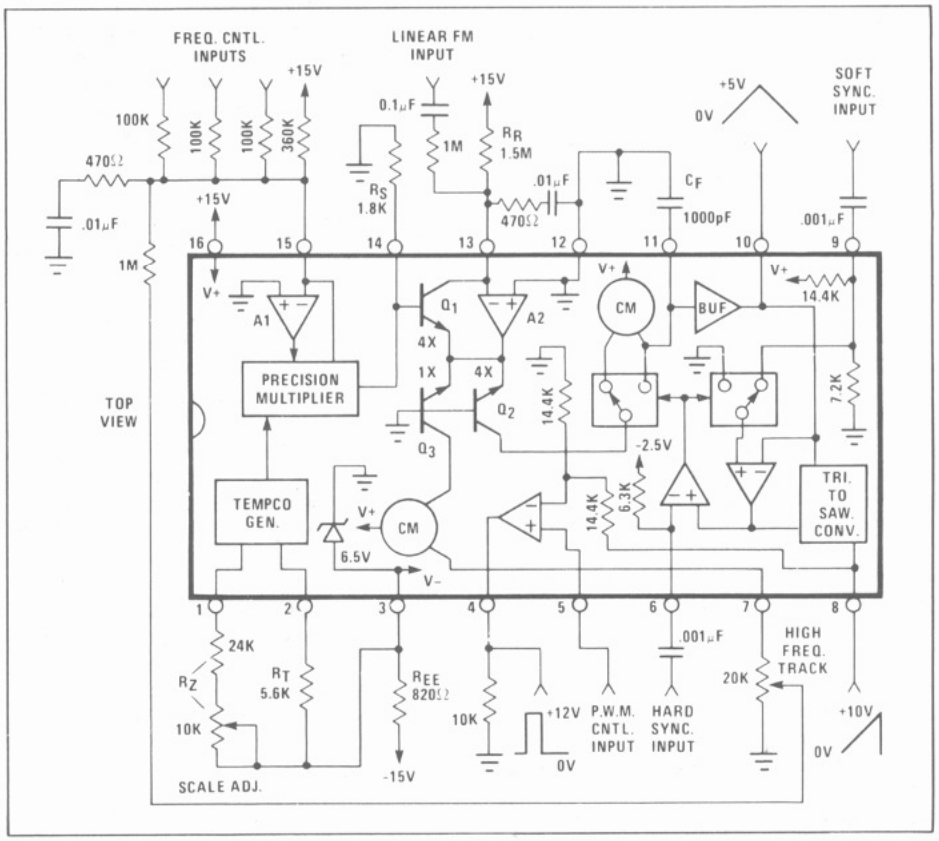
The CEM 3340 and CEM 3345 are completely self contained, precision voltage controlled oscillators, featuring both exponential and linear control scales and up to four buffered output waveforms: triangle, sawtooth, square, and pulse with voltage controllable pulse width. Full temperature compensation makes these VCOs extremely stable, and eliminates the need for a temperature compensation resistor. The highly accurate exponential and linear control inputs are virtual ground summing nodes, allowing multiple control voltages to be mixed within the device itself.

Also included is provision for hard and soft synchronization of the frequency, and an output for easy adjustment of high frequency tracking. Special care in the design ensures oscillation start-up under any power-on sequence and supply conditions.

Although a low voltage process has been used to reduce die size, cost, and leakage currents, an on-chip 6.5 volt zener diode allows the device to operate off ±15 volt supplies, as well as +15,-5 volt supplies.



CEM 3340 Circuit Block and Connection Diagram



Features

- Large Sweep Range: 50,000:1 min.
- Fully Temperature Compensated; No Q81 Resistor Required
- Four Output Waveforms Available; No waveform trimming required.
- Summing Node Inputs for Frequency Control
- High Exponential Scale Accuracy
- Low Temperature Drift
- Voltage Controlled Pulse Width
- Hard and Soft Sync Inputs
- Linear FM
- Buffered, Short Circuit Protected Outputs
- ±15 Volt Supplies

Electrical Characteristics

V_{CC} = +15V V_{EE} = Internal Zener T_A = 20°C				
Parameter	Min.	Typ.	Max.	Units
Frequency Control Range	50K:1	500K:1	–	
Exponential Scale Error, Untrimmed[1]	–	0.2	1	%
Exponential Scale Error, Trimmed[1]	–	0.05	0.3	%
Multiplier Gain Error[2]	–	0.0005	0.008	%/μA
Tempo Cancellation[3]	-150	0	+150	ppm
Oscillator Drift[4]	–	±50	±200	ppm
Triangle Buffer Input Current	–	0.3	3	nA
Triangle Waveform Upper Level	4.85	5.0	5.15	V
Triangle Waveform Lower Level	-15	0	+15	mV
Triangle Waveform Symmetry	45	50	55	%
Sawtooth Waveform Upper Level	9.4	10.0	10.6	V
Sawtooth Waveform Lower Level	-25	0	+25	mV
Triangle Output Sink Capability	400	550	750	μA
Sawtooth Output Sink Capability	640	800	1000	μA
Triangle & Sawtooth Output Impedance[5]	65	100	150	Ω
Pulse Output Source Capability at +10V	2.8	3.5	4.6	mA
Squarewave Output Levels[6], CEM 3345	-1.8,-0.4	-1.3,0	-0.8,+0.4	V
PWM Input Pin Current[7]	.5	1.5	3.5	μA
PWM Input Voltage for 0% Pulse Width	-15	0	+15	mV
PWM Input Voltage for 100% Pulse Width	4.6	5.0	5.4	V
Input Bias Current at Reference and Control Current Inputs	80	200	400	nA
Tempco of Input Bias Currents	-1000	0	+1000	ppm
Offset Voltage at Reference and Control Current Inputs	-5	0	+5	mV
Hard Sync Reference Voltage	-2.3	-2.5	-2.8	V
Hard Sync Input Resistance	5	6.3	7.9	KΩ
Max Capacitor Charge/Discharge Current	400	570	800	μA
Positive Supply Current	4	5	6.5	mA
Positive Supply Voltage Range	+10		+18	V
Negative Supply Voltage Range[8]	-4.5		-18	V

Note 1: This error represents the percentage difference in scale factors (volts per frequency ratio) of the exponential generator anywhere over the exponential generator current range of 50nA to 100μA. Most of this error occurs at the range extremities.

Note 2: This error represents the percentage difference in multiplier gains at any two input currents, within the range of 20 μA to 180 μA, per μA difference between the two corresponding outputs.

Note 3: This spec represents the difference between the actual tempco of the multiplier output voltage (expressed relative to the maximum output excursions) and the tempco required to precisely cancel the tempco of the exponential scale factor (q/KT).

Note 4: The multiplier output is grounded.

Note 5: For exponential generator currents less than 10 μA; above 10 μA, impedance drops to 1/3 this value as the highest current is approached.

Note 6: With respect to the hard sync input reference voltage.

Note 7: For PWM control inputs between -1 and +6 volts. This current is significantly greater for inputs outside of this range.

Note 8: Current limiting resistor required for negative supplies greater than -6 volts.

Application Hints

Supplies

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% Zener diode has been provided to allow the chip to operate off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 3). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 3 and the negative supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2) / .008$$

Although the circuit was designed for a positive supply of +15 volts, it may be operated anywhere between +10 and +18 volts. The only effect is on the positive peak amplitude of the output waveforms in accordance to the following: The triangle peak is one third of the supply, the sawtooth peak is two thirds of the supply, and the pulse peak is 1.5 volts below the supply.

Operation of the Temperature Compensation Circuitry

The exponential generator is temperature compensated by multiplying the current sourced into the frequency control pin (pin 15 on the CEM3340, pin 17 on the CEM3345) times a coefficient directly proportional to the absolute temperature. As this control current is applied to the exponential generator, its coefficient cancels that of the exponential generator, q/KT. This coefficient is produced by the tempco generator using the same mechanisms that create it in the exponential generator; cancellation is therefore nearly perfect.

The output of the precision multiplier (pin 14 on the 3340,

pin 16 on the 3345) internally connects to the control input of the exponential generator (base of Q_1). This output is a current and is given by:

$$I_{OM} = \frac{22V_T}{R_T}(1 - I_C R_Z/3.0)$$

where $V_T = KT/q = 26$ mV @ 20°C, and where I_C is the total current flowing into the frequency control pin and must remain positive for proper operation (a negative input current will produce the same output as a zero input current). Since the frequency control input pin is a virtual ground summing node, any number of control voltages may be summed simply with input resistors to this pin.

The current output of the multiplier is converted to the required drive voltage with a resistor from the multiplier output pin to ground. For greatest multiplier accuracy, this resistor, R_S, should be 1.8k and the current flowing out of pin 2, $22V_T/R_T$, should be close to the current flowing out of pin 1, $3.0/R_Z$.

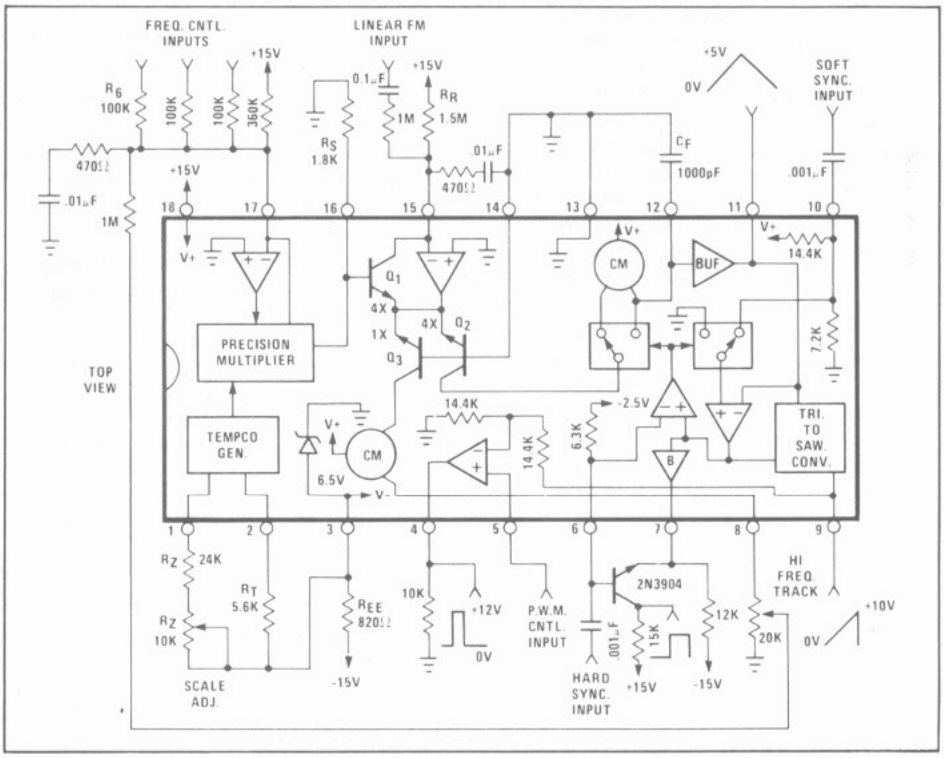
Since the components associated with the tempco generator and multiplier determine the maximum voltage excursion possible at the base of Q_1, they should be selected to provide the desired frequency control range of the oscillator. The exponential generator itself is capable of delivering a current for charging and discharging the timing capacitor from greater than .5mA down to less than the input bias current of the buffer, thus allowing for a typical frequency range greater than 500,000:1. The most accurate portion of this current range, from 50nA to 100μA, should be used for the most critical portion of the desired frequency range.

Consideration of this critical range determines the value of

Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	+24V,-0.5V
Voltage Between V_{CC} and Ground Pins	+18V, -0.5V
Voltage Between V_{EE} and Ground Pins	-6.0V,+0.5V
Voltage Between Frequency Control Pin or Reference Current Pin and Ground Pin	±6.0V
Voltage Between Multiplier Output Pin and Ground Pin	+6.0V, -1V
Current through Any Pin	±40mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-25°C to +75°C

CEM 3345 Circuit Block and Connection Diagram



C_F, the timing capacitor. The oscillation frequency is given by:

$$f = 3\, I_{EG}/(V_{CC}\, C_F)$$

where I_{EG} is the output current from the exponential generator. If, for instance, the most important frequency range is from 5Hz to 10kHz, then C_F should be 1000pF at V_{CC} = +15V (a low leakage, low tempco capacitor, such as mica, should be used for C_F).

Next the reference current for the exponential generator (Current into pin 13 on the 3340, pin 15 on the 3345) is selected. This current ideally should be the geometric mean of the selected generator current range, but consideration of the temperature coefficient of

the bias current for op amp A2 usually dictates a higher value for the reference current. Although this bias current has been temperature compensated, it could have a worst cast tempco of 1000ppm and maximum value of 400nA. Under these conditions, a reference current of 10μA through Q_1, for instance, would have a tempco of 40ppm. It is recommended that, in general, the reference current be selected in the 3μA to 15μA range.

Since the reference current pin is a virtual ground summing node, the reference current may be set up with a temperature stable resistor to V_{CC}, or other positive stable voltage source. A negative current into this pin will simply gate the exponential generator completely off.

With the value of C_F and reference current now selected, the voltage excursion at the multiplier output, which drives the base of Q_1, is now determined for the desired frequency control range. If this range were 1Hz to 20kHz, the exponential generator current, I_{EG}, would have to range from 10nA to 200μA in the above example, requiring the base drive voltage, V_B, to vary from +180mV to -78mV, since

$$I_{EG} = I_{REF}\ e^{-V_B/V_T}$$

The most positive voltage at the base of Q_1 occurs when the control current, I_C, is zero, and is $22V_T\ R_S/R_T$. Therefore, in the above example, $R_T = 22V_T \cdot 1.8K/.18V = 5.72K$, and $R_Z = 3.0R_T/22V_T = 30K$ nominal. Finally, since the multiplier output current must range from +100μA to -43μA to produce this desired voltage excursion at the multiplier output and on the base of Q_1, the control input current, I_C, ranges from 0 to 143μA. A resistor from V_{CC} to the control input pin may be used to set the oscillator frequency at some initial value with no control voltages applied.

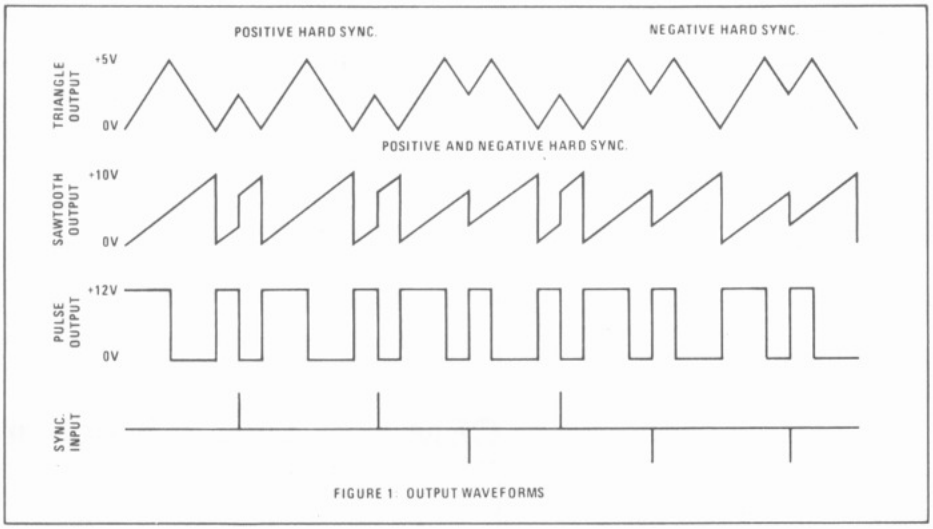


FIGURE 1. OUTPUT WAVEFORMS

The frequency control scale is determined by the value of the input resistor to the control pin, the value of the Q_1 base resistor, R_S, and the multiplier current gain. Since the multiplier current gain, set by the ratio of the pin 2 current to pin 1 current, should be near unity and R_S should be 1.8K, the control input resistor is the component which should be selected for the desired control scale. For the industry standard scale of 1 octave/volt, the input summing resistors become 100k. The recommended method for trimming the control scale is to tweek the multiplier current gain by adjusting the value of R_Z ±20% about the nominal value.

Both the multiplier and the exponential generator are compensated with the 470Ω - .01μF networks shown in the Block Diagrams and are therefore necessary in any application. Since the bandwidth of the multiplier extends beyond the audio range, it may be desirable to limit the bandwidth to reduce possible noise at the base of Q_1, thereby reducing FM noise and frequency jitter. This is best accomplished by bypassing R_S to ground with a capacitor, where the corner rolloff frequency is given by: $f_{LP} = 1/(2\pi R_S C)$.

Trimming The Scale Error

There are two basic sources producing exponential conformity error in the control scale: One is the exponential current generator and the other is the precision multiplier.

The error from the exponential converter is due partly to the bulk emitter resistance of Q_2, becoming significant at generator currents greater than 100μA, and partly to the comparator switching delay, becoming significant at frequencies greater than 5KHz. These two effects cause the oscillator frequency to go flat, but only at the uppermost octaves.

Circuitry has been provided to correct for these effects. The output of the hi-frequency track pin (pin 7 on the 3340, pin 8 on the 3345) is a current which is one fourth the generator output current, I_{EG}. This current may be converted with a grounded resistor to a voltage, a portion of which is

then fed back to the control input pin. As the frequency is increased, this feedback voltage will tend to sharpen the control scale, but only at the upper end, since the feedback voltage becomes significant only at the higher generator currents. The amount of voltage fed back is adjusted so the scale is sharpened just enough to compensate for the inherent high end flatness

The method recommended for trimming the control scale is as follows: The hi-frequency track adjust is first set so that no correction voltage is fed to the control input. The oscillator frequency is set around 200Hz and the scale adjust trimmer is adjusted for the desired scale factor (e.g. 1.000 octave/volt). Then the oscillator frequency is set to around 10KHz, and the hi-frequency track trimmer is adjusted for the same scale factor.

The source of error from the precision multiplier is due to the multiplier's gain (nominally unity) changing as the control input current changes. This type of error causes the frequency to become increasingly sharp or flat as the control current is increased. The percentage difference in multiplier gains, and hence scale factors, at any two inputs to the multiplier may be calculated as the percentage error given in the specifications times the difference in μA between the two corresponding outputs. For example, suppose the scale were adjusted for precisely 1 octave/volt at midrange. At one octave above this adjusted octave, with the multiplier output 10μA different, the scale factor could be .08% different worst case. This would produce a volts/octave error at the base of Q_1 of .08% x 18mV = 14.4μV, which would cause this octave to be .06% (1 cent) sharp or flat. At five octaves above the adjusted octave, the scale factor could be 0.4% different worst case, producing a volts/octave error of 0.4% x 18mV = 72μV. This fifth octave would thus be 0.28% (5 cents) sharp or flat. Note that if octaves above the adjusted octaves were sharp, those octaves below the adjusted octave would become increasingly flat, and vice versa.

Typically the error produced by the multiplier is much less than the above example. However, if maintaining a tighter tolerance is required for the particular application, the multiplier error may be trimmed out for each device. The trimming procedure requires that both R_Z and R_S be made adjustable ±30% about the nominal value; R_Z is first adjusted so that the multiplier gain is constant over the selected input current range; then R_S is adjusted for the desired scale factor (adjusting R_S will reintroduce some error, so R_Z may have to be readjusted).

Should for some reason it be desired not to use the temperature compensation circuitry, the multiplier/tempco generator may be bypassed simply by leaving pin 1, pin 2, and the control input pin open, and applying the control voltage to the base of Q_1 via the multiplier output pin.

Waveform Outputs

All waveform outputs are short-circuit protected and may be shorted continuously to any supply without damaging the device. Each output, however, has differing drive capabilities.

Although the triangle output can sink at least .4mA and source over several mA, care must be exercised in loading this output. Because the output has a finite impedance and drives the comparator, a change in load will change the frequency of the oscillator. Adding a 100K resistor to ground, for instance,

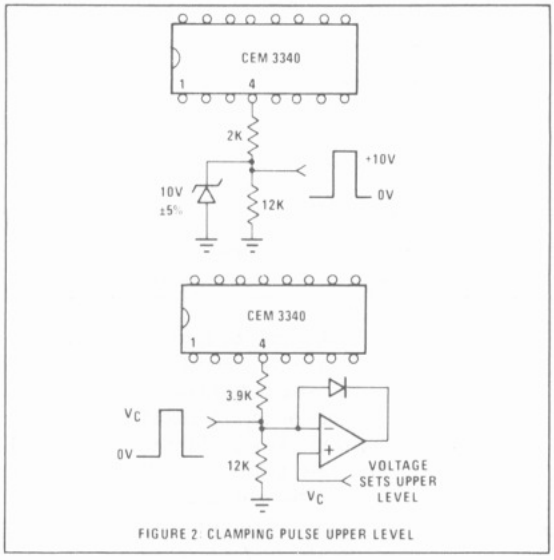


FIGURE 2: CLAMPING PULSE UPPER LEVEL

could lower the frequency by 150/100K = 0.15% (2.5 cents) worst case. A load capacitance will act like a resistor with a value $1/(2fC_L)$ and requires the same considerations as above. A continuous load no greater than 10K and/or 1000pF to ground is recommended.

Since the sawtooth output is buffer isolated from the oscillator circuitry, it can sink at least .6mA and source over several mA with no effect on oscillator performance, and only negligible effect on sawtooth waveshape. Stray capacitance at this output greater than 40pF, however, will cause a small high frequency oscillation. A 100Ω resistor between the output and load is all that is required to isolate more than .01μF.

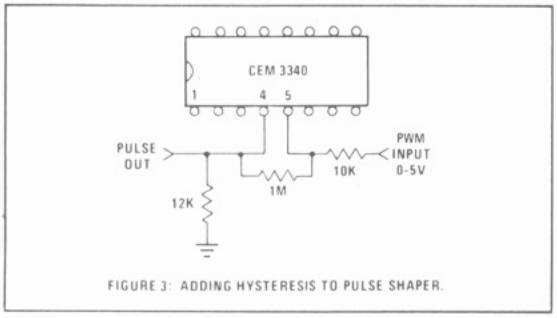


FIGURE 3: ADDING HYSTERESIS TO PULSE SHAPER.

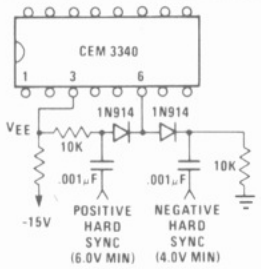


FIGURE 4: METHOD FOR SYNC ON RISING OR FALLING EDGE.

The pulse output is an open NPN emitter, and therefore requires a pull-down resistor to ground or to any negative voltage. Any pull-down voltage between ground and .5 volt above the voltage on the negative supply pin will precisely determine the lower level of the pulse wave. For pull-down voltages more negative than this, the lower level will be nearly the negative supply pin voltage. The nominal upper level of the pulse wave is given by: V_{CC} - 0.3V -1.3K · I_{PLD} for $I_{PLD} >$ 0.6mA, and V_{CC} - 0.9V for $I_{PLD} <$ 0.6mA, where I_{PLD} is the pull down current. A maximum value of 3mA for I_{PLD} is recommended. For those applications which require a more stable, well defined upper level, the circuits shown in Figure 2 may be used.

The pulse width of the pulse output may be set from 0 to 100% with a 0 to +5V external voltage (V_{CC} = +15V) applied to the PWM control input pin (pin 5 on the 3340 and 3345). The fall time of the pulse wave is slower than the rise time due to finite comparator gain. It may be speeded up considerably by adding hysteresis as shown in Figure 3. Care should be exercised in the layout to prevent stray capacitive coupling between the pulse output and the PWM input,as this can cause comparator oscillation.

The square wave output (pin 7) from the CEM 3345 also requires a pull down resistor to any negative supply greater than -4 volts. It provides an output swing from nominally 1.3 volts below the hard sync reference voltage to a level nominally the same as the hard sync reference voltage. The Block Diagram shows a convenient way of generating a full swing square wave from this output. The current pulled down from this output should also be limited to a maximum of 3mA.

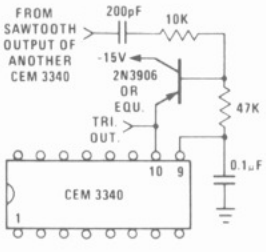


FIGURE 5: CONVENTIONAL HARD SYNC

Frequency Synchronization

The oscillator frequency may be hard synchronized in several different ways. One way is to couple positive pulses, negative pulses, or both, into the hard sync input pin (pin 6 on the 3340 and 3345). A positive sync pulse will cause the triangle wave to reverse directions only during the rising portion of the triangle, while a negative sync pulse will cause direction reversal only during the falling portion. The resulting waveforms are shown in Figure 1, and provide a wider variety of synchronized sounds than possible through conventionally synchronized oscillators. Simple capacitive coupling as shown in the Block Diagrams allows hard synchronization on both the rising and falling edge of a rectangle wave. Figure 4 shows circuitry for allowing only one or the other of the edges to synchronize the oscillator. The peak amplitude of the pulses actually appearing on the sync pin should be restricted to 1 volt minimum and 3 volts maximum for best operation.

Another method of hard synchronizing the oscillator is shown in Figure 5. Negative pulses only are coupled into the base of the PNP transistor, with a peak amplitude of 8 to 10 volts for best results at V_{CC} = +15V. This method will produce the same waveforms generated by the conventionally synchronized sawtooth oscillators.

Finally, the oscillator may be soft synchronized by negative pulses applied to the threshold voltage pin (pin 9 on the 3340, pin 10 on the 3345). These pulses cause the triangle upper peak to reverse direction prematurely, causing the oscillation period to be an integral multiple of the pulse period. The peak amplitude of these negative pulses should be limited to 5 volts maximum and positive pulses should be avoided entirely. If this input is not used for synchronization purposes, it is recommended that it be bypassed with a 0.1μF capacitor to ground to prevent synchronization or jitter to noise pulses on the V_{CC} supply line.

Linear FM

The reference current input pin may be used for linear modulation of the frequency. The external input is summed with the reference current simply through a resistor terminating at this pin. For audio FM, it is recommended that a coupling capacitor be used to prevent frequency shift when connecting to the external source. The value of the input resistor should be selected so that the maximum peak to peak input signal produces a plus and minus current equal to the reference current.

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C E M 3 3 6 0

DUAL VOLTAGE CONTROLLED AMPLIFIER

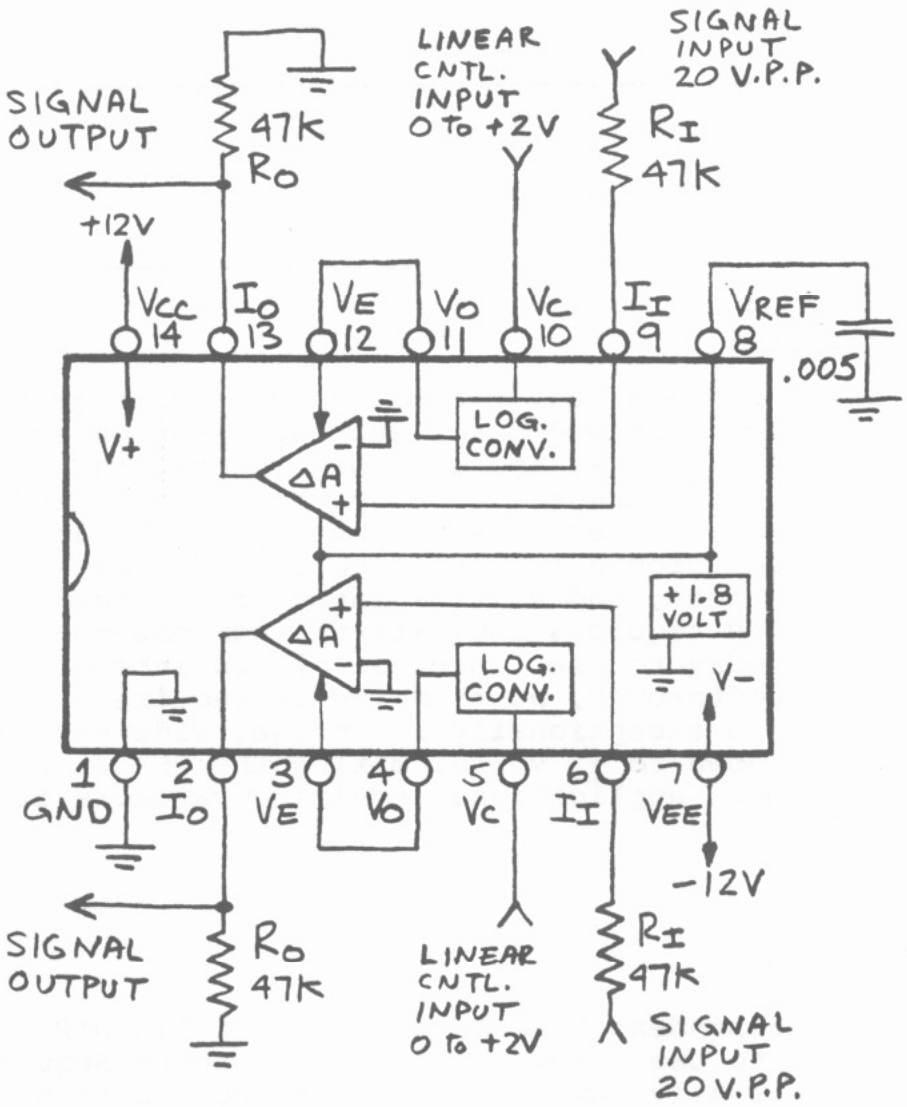
Preliminary, January 1981

Description:

The CEM 3360 is a dual general purpose voltage controlled transconductor intended for such application as voltage controlled amplifiers, filters, and waveform generators. Each transconductor independently provides both linear and exponential control scaling over greater than a 100 dB range. Complete with virtual ground summing inputs, wide voltage compliance current outputs, and control inputs referenced to ground, the CEM 3360 requires few external components and it is extremely easy to use. Because of its inherent ultra-low control feedthrough, no trimming is required. Added to these features are exceptionally low noise, wide bandwidth, and operation down to ±3 volts, making the CEM 3360 a real cost saver in most applications requiring variable transconductance amplifiers.

Features:

- Low Cost
- Two Independent VCAs in a Single 14 Pin DIP
- Simple to Use - Few External Components Required
- Exceptionally Low Control Feedthrough Without Trimming: 10mV Max. out of 10 V.P.P. Output
- Low Noise: -100 dB Typical
- No Trimming Required
- Summing Node Signal Inputs
- Current Outputs Capable of Swinging to Within 1.5V of Each Supply
- Linear and Exponential Control
- Control Voltages Referenced to Ground
- Wide Supply Range: ±3 to ±12 OR +15, -3 to -9 Volts



CEM3360 BLOCK DIAGRAM AND TYPICAL CONNECTION

Specifications, CEM 3360

V_{CC} = +12V V_{EE} = -12V

Parameter	Min	Typ	Max	Units
Control Range, Linear & Exponential	100	--	--	dB
Control Scale Sensitivity				
Exponential[1]	2.7	3.0	3.3	mV/dB
Linear	48	52	56	%/V
Tempco of Control Scales				
Exponential	+3000	+3300	+3600	ppm
Linear	---	± 250	± 750	ppm
Control Scale Error				
Exponential[1]	---	0.6	2	dB
Linear[2]	---	3.0	6.0	%
Maximum Cell Current Gain[3]	.9	1.0	1.1	
Maximum Signal Input & Output Current	± 300	± 400	± 500	uA
Signal Input Offset	+10	0	-10	mV
Control Feedthrough Without Trim[4]	---	±.07	±.3	uA
Total Harmonic Distortion[3]	---	1.0	3.0	%
Output Noise[5]	---	.4	1.2	nARMS
Signal Attenuation @ Linear V_C=0[6]	70	80	---	dB
Linear Control Voltage for Max Gain	1.79	1.93	2.08	V
Output Impedance[3]	5	12	---	MΩ
Output Voltage Compliance[3]	V_{EE}+1.2		V_{CC}-.8	V
V_{REF}	1.75	1.8	1.85	V
Control Input Bias Current				
Exponential[3]	.3	.8	1.5	uA
Linear	.5	1.6	4	uA
Supply Current				
Positive	3.8	4.8	6.0	mA
Negative	3.8	4.8	6.0	mA

Specifications, CEM 3360

Parameter	Min	Typ	Max	Units
Signal Current Bandwidth	2.0	5.0	---	MHz
Signal Current Slew Rate[3]	0.5	1.5	---	mA/uS
Crosstalk Between VCAs[7]	-80	-90	---	dB
Positive Supply Range[8]	3.0	---	18	V
Negative Supply Range[8]	-3.0	---	-18	V

NOTES:

1. Current gain is -20dB to -80dB
2. Best straight line. Most of this error occurs at range extremities. See Hints.
3. Output Signal Current is ±100uA.
4. Over entire control range. Signal input is open.
5. In 16 to 16KHz bandwidth.
6. For negative supply less than 12 volts, this attenuation is greater. See Hints.
7. At 1KHz.
8. Total supply voltage across chip should not exceed 26V.

Supplies

Both positive and negative supplies may range from 3 to 18 volts with little effect on performance. The total supply across the chip (V_{CC} - V_{EE}), however, should be maintained less than 26 volts. This allows such standard supplies as ±12 volts, +15, -5 volts, +5, -12 volts to be used with guaranteed reliability. Greater supplies up to 32 volts, such as ±15 volt supplies, may be used but with an occasional device exhibiting junction breakdown. No guarantee is made for devices operated over a total supply of 26 volts.

Basic Operation

Each of the two voltage controlled transconductors consists of a non-inverting current attenuator with a near exponential control scale (see Control Inputs) and an isolated log converter. When the outpt of the log converter is connected to the exponential control input of the current cell, as shown in the Block Diagram, the composite control response becomes linear. The signal input, like the output, is a current and accepts input currents of either polarity; the cell current gain reaches a maximum of nominally unity and may be decreased to less than -100dB with the control input.

Since the signal input is at a voltage within 10mV from ground, it may be considered for all practical purposes as a virtual ground summing node. Thus, an input voltage may be converted to the required input current with a single input resistor, and multiple input signals may be mixed with multiple input resistors connected to the input pin, as shown in Figures 1 and 2. In actuality, the signal input does not exhibit the ideal zero ohm input impedance, but instead looks like a 900 resistor in series with forward conducting diodes. Thus, a ±100 uA input current produces approximately ±200mV at the input pin.

The output of each cell is a high impedance current output, able to drive into voltages within 1.2 volts of the negative supply and .8 volts from the positive supply. Thus, the current output may be converted to a voltage simply with a resistor to ground; if necessary the output may then be buffered with an op amp follower to provide a low output impedance drive. Such a non-inverting configuration is shown in Figure 1.

Alternatively, the current outputs may drive the summing input of an op amp inverter to provide an inverting configuration, as shown in Figure 2.

Selection of Component Values

The values for the input and output resistors (or feedback resistor in the case of the inverting configuration) depends on the abailable input voltage, desired maximum output voltage,

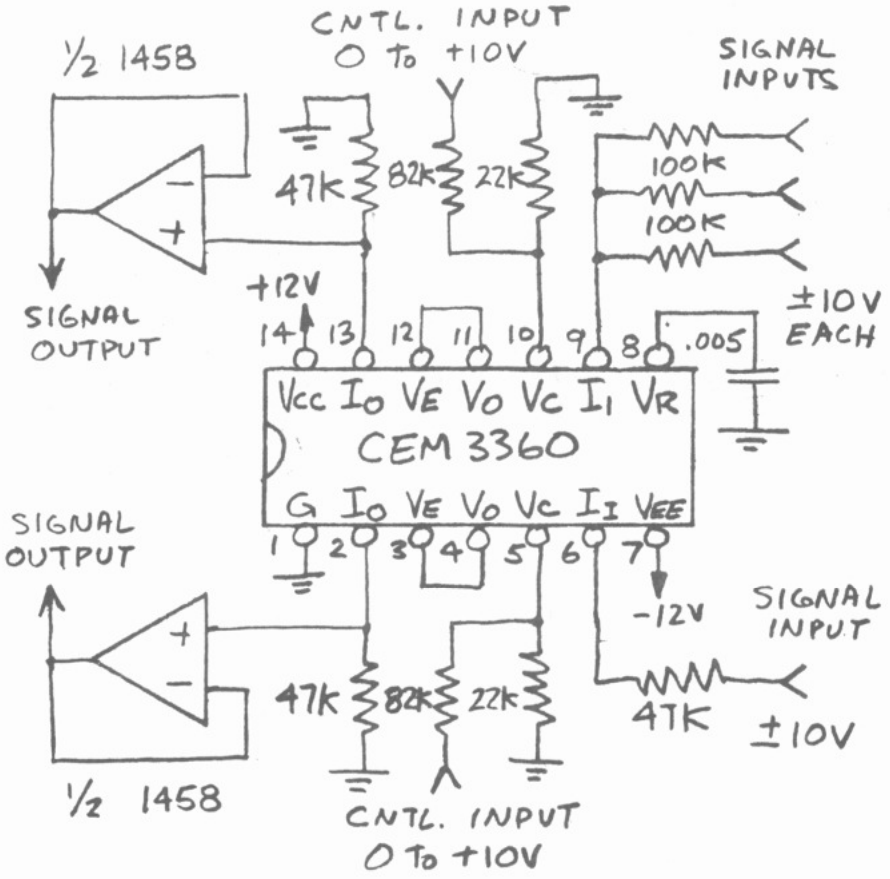


FIGURE 1: NON-INVERTING CONNECTION, LINEAR CONTROL SCALE

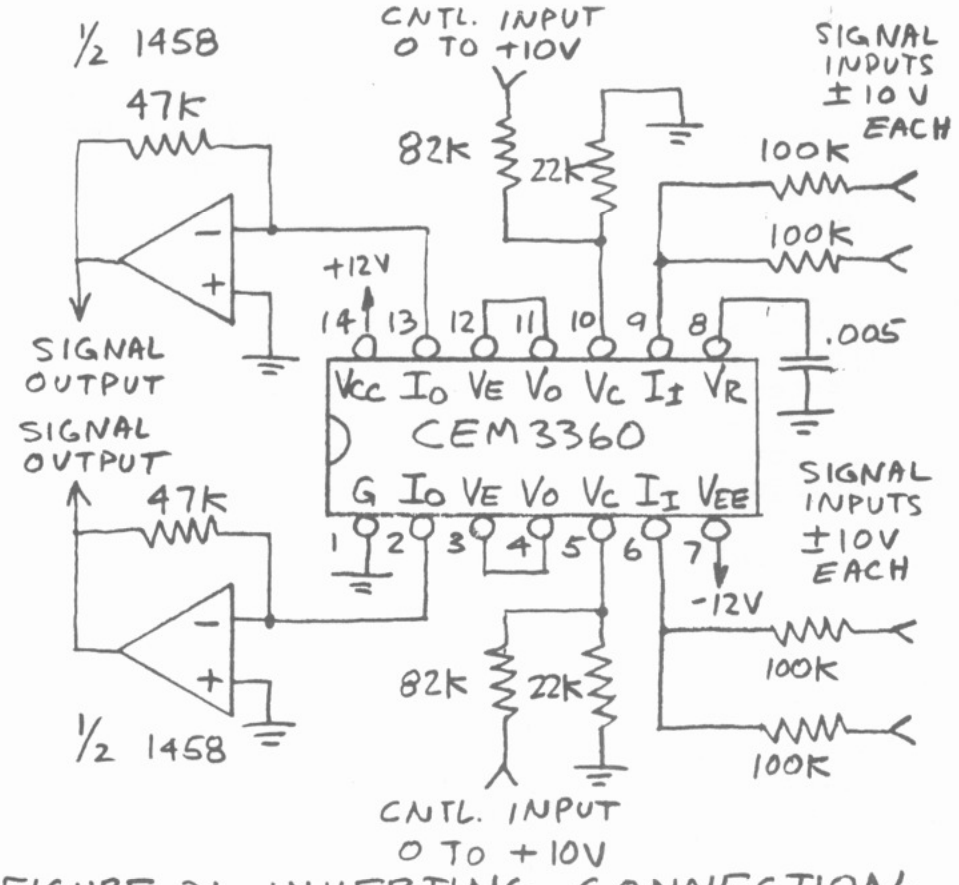


FIGURE 2: INVERTING CONNECTION, LINEAR CONTROL SCALE

and to some extent, what parameters are more important.

The specification for maximum input and output current is the maximum positive input current which the device input can handle; positive currents above this value will be hard limited and thus severely distorted.

Hence, it is recommended that for best signal to noise ratio and minimum feedthrough relative to the maximum output, the input resistor, or resistors, should be selected so that the total peak input current is in the 200 - 300 uA range. However, for applications where distortion is more important, the inputs should be operated nominally somewhat lower, around 100 uA.

For resistor value calculation purposes, the input may be assumed to be a virtual ground summing node if the input voltage is above several volts. For lower input voltages, the following equation may be used to calculate the input resistor, or resistors:

$$R_{IN} = \frac{V_{IN} - 120\ mV}{I_{IN}} - 900$$

V_{IN} is the available input voltage while I_{IN} is the selected input current, typically 100 - 300 uA. Note that signals 400mV or less peak may be applied directly to the input pin. For best distortion performance, however, the input voltage should be maintained as large as possible and an input resistor used.

The value of the output resistor, or feedback resistor, is then selected to give the maximum desired output voltage with the particular input voltage. With the control inputs set for maximum gain, the current gain is unity; a ±100uA input, for instance, will produce a nominal maximum output of ±100uA. Note that while the maximum current gain possible is unity, the maximum voltage gain can be either greater or less than unity.

The Control Inputs

Each transconductor may be connected to provide either a linear control response or an exponential control response.

For a linear control response, the V_O pin (output of the log converter) is hardwired to the V_E pin (exponential control input to the variable gain cell), and the control voltage is applied to the V_C pin (input to the log converter).

The control voltage range to this input is from nominally zero volts for minimum gain to nominally 1.93 volts for maximum gain. Since this input is a relatively high impedance, a resistor divider may be used to accommodate a larger control range, 0 to +10 V for instance. The resistor divider impedance

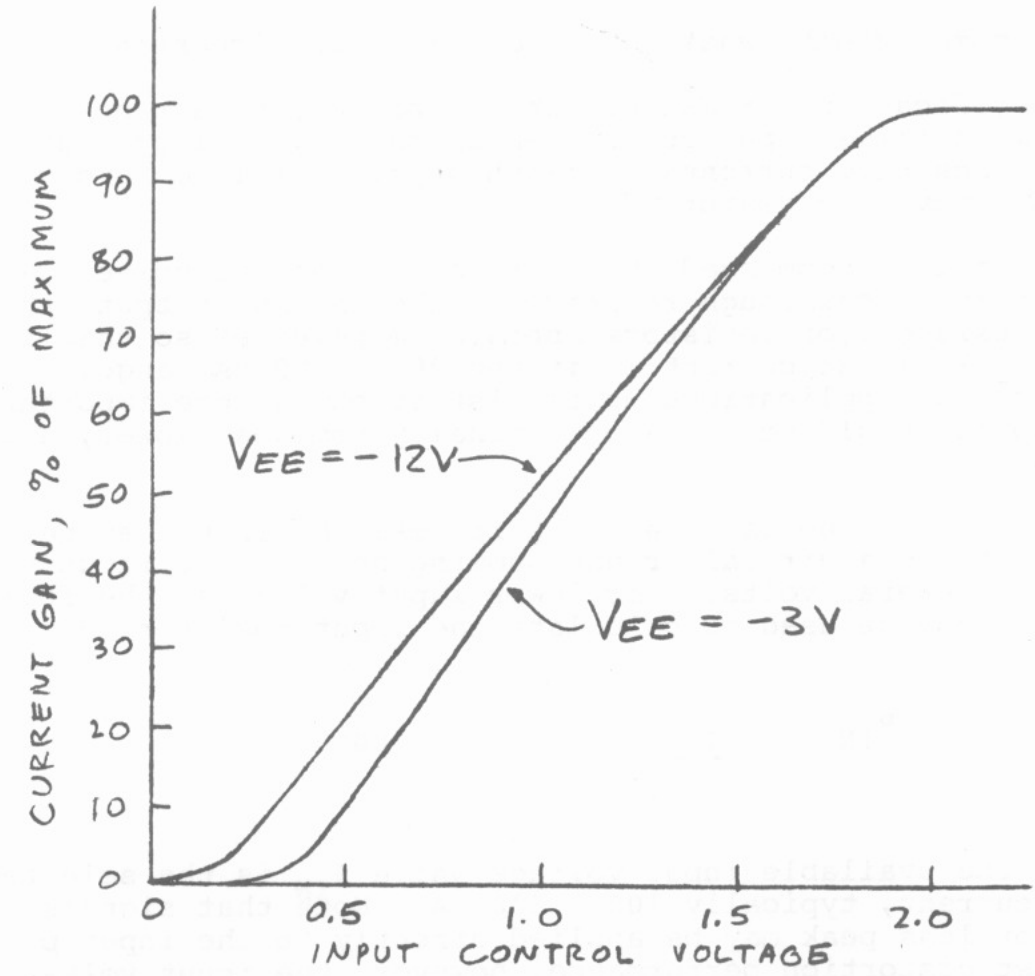


FIGURE 3: LINEAR CONTROL RESPONSE

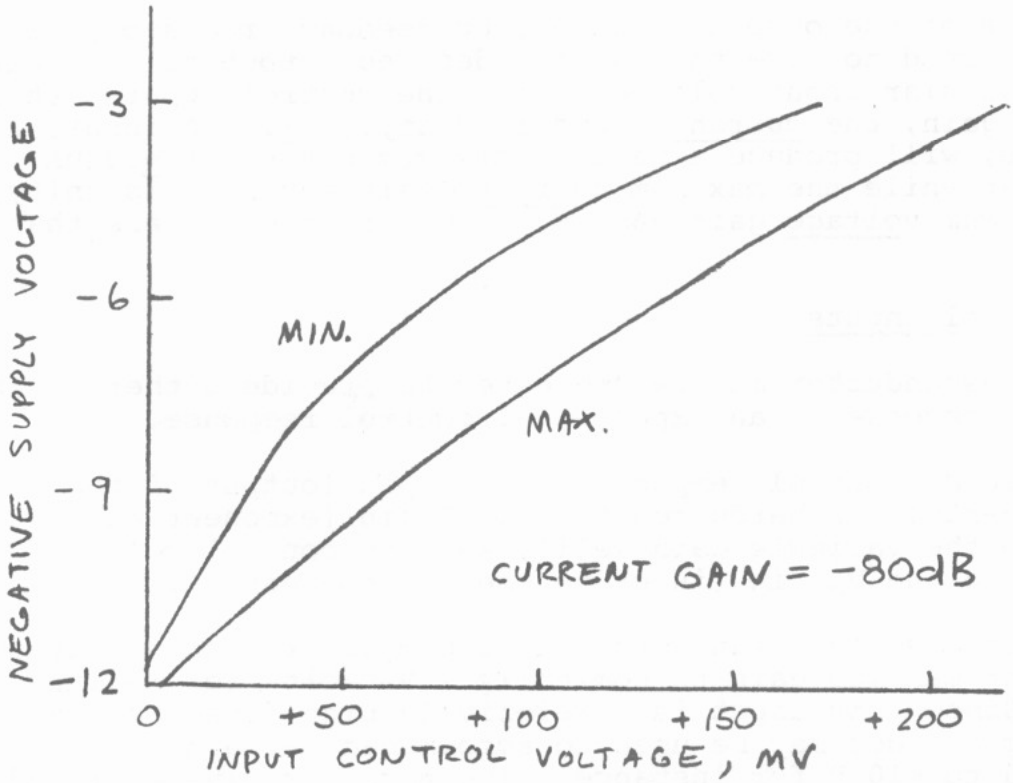


FIGURE 4: TURN-ON THRESHOLD, LINEAR INPUT

at the V_C pin should be kept less than 50K to minimize control input loading errors. Typical external connections for a linear response is shown in Figures 1 and 2.

Figure 3 shows the typical response of gain versus control voltage for the linear control input. As can be seen, this response curve is not perfectly linear, but has a rounded knee at the very beginning and at the very end. In addition, for negative supply voltages less than -12 volts, there is a small positive threshold which must be overcome before the cell gain begins to increase at all; at -3 volts, this threshold is typically +180 mV. Thresholds at other negative supply voltages are given in Figure 4. If an application at negative supplies less than -12 volts requires this turn-on threshold to be minimized, than a positive offset equal to the minimum threshold shown in Figure 4 can be built into the control circuit. In the circuits of Figures 1 and 2, for instance, this offset can be added simply with a resistor from the V_C pin to the positive supply voltage.

To provide an exponential control response, the log converter is not used at all (the V_C and the V_O pins may be simply left open) and the control voltage is applied directly to the V_E pin. In Figure 5 is shown the typical response of cell current gain in dB versus the voltage on pin V_E with respect to the reference voltage, V_{REF}, on pin 8. As can be seen, the exponential conformity is very good from -90dB to -20dB, corresponding to a control voltage of 270mV to 60mV below the reference voltage, nominally 1.8V. For the last 20dB of attenuation, corresponding to -60mV to +60mV with respect to V_{REF}, the transfer curve is quite rounded.

A typical circuit connection for an exponential control response is shown in Figure 6. For best gain consistency from device to device, the input resistor divider is referenced to the reference voltage on pin 8. The resistor ratio is selected such that with a control voltage of zero, the voltage appearing on the V_E pin is 240 mV below V_{REF}, and the corresponding current gain is -80dB.

On the linear portion of the curve, the gain will increase 20dB for approximately every 450mV increase in control voltage; maximum gain (0 dB) will occur at approximately +2.2 volts. A wider control input range may be accommodated by adding a resistor from the V_E pin to the negative supply and ratioing the resistors so that the input voltage range produces the desired voltage excursion on the V_E pin.

The impedance of the resistor network at the V_E pin should be kept below 5K to minimize loading errors by the V_E pin. Also, care should be exercised to ensure that the resistor networks connected to pin 8 do not source more than a total of 400uA or sink more than a total of 1mA from this pin.

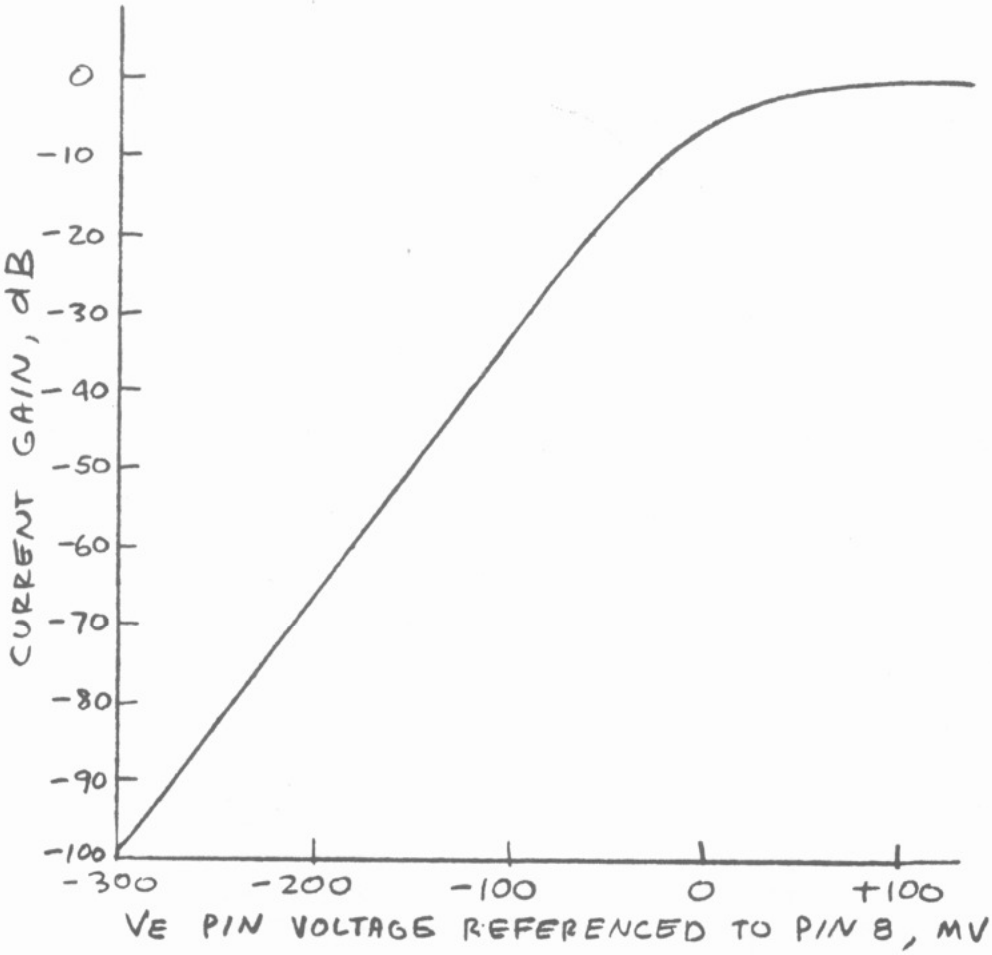


FIGURE 5: EXPONENTIAL CONTROL RESPONSE

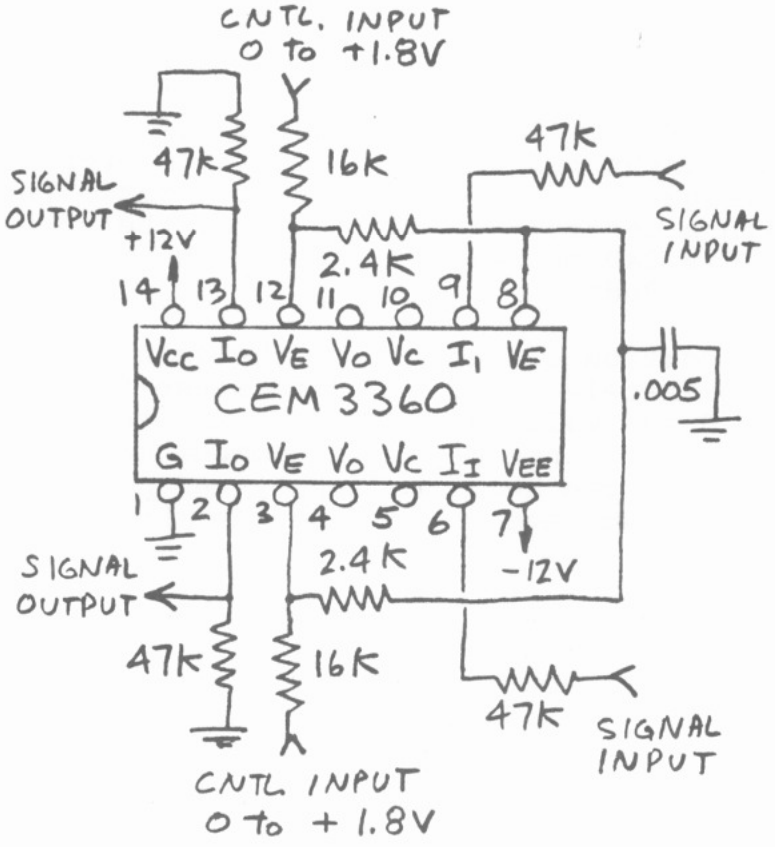


FIGURE 6: CONNECTION FOR EXPONENTIAL CONTROL SCALE

Trimming the Control Feedthrough

Although the worst case control feedthrough of the CEM3360 without trimming is sufficiently low for the vast majority of applications, some applications may require even lower feedthrough. The control feedthrough may be improved by at least a factor of 10 by injecting a small bipolar current (±2uA) into the signal input and adjusting its value until there is zero output current when the gain is set for maximum. This method of feedthrough trimming is shown in Figure 7.

A potential source of feedthrough in addition to that specified in the specifications is the signal input offset voltage. Even though the voltage applied to the input resistor may be at ground potential (zero volts), a small current may flow into the input due to an offset voltage at the input pin; this in turn will cause an output offset at maximum gain. If, for instance, the input and output resistor are equal valued and the input resistor is connected to ground, a 5mV input offset will produce 5mV of control feedthrough as the gain is varied from minimum to maximum.

The simplest way to eliminate this source of feedthrough is to capacitively couple to the signal input. For direct coupled inputs, the resulting control feedthrough may be trimmed out by using the method of Figure 7. The injected current, however, should then range over the worst case input offset divided by the input resistor value, or $I_{TRIM} = \pm 10mV/R_{IN}$.

It should be pointed out that this source of feedthrough is only a problem for small input resistors or maximum voltage gains greater than unity. Otherwise, the feedthrough produced by input offset is on the same order or less than the inherent feedthrough.

Other Applications

The flexibility and simplicity of the CEM3360 lends itself to numerous applications other than VCA's: V.C. (Voltage Controlled) filters, V.C. timers, V.C. pulse delay, V.C. resistors, V.C. lag processors, V.C. sine wave oscillators, and V.C. waveform generators, to name only a few. Shown in Figure 8 is one such application in a waveform generator.

This generator features two waveforms with adjustable shape. The output of A1 can be adjusted from rising ramp to triangle to falling ramp, while the duty cycle of the comparator A_2 output can be varied from 5% to 95%. The frequency can be swept over greater than a 10,000:1 range with a 0 to +2 volt control input; the control scale is roughly one decade per half volt. The capacitor can be selected for either the subaudio (LFO) or audio range.

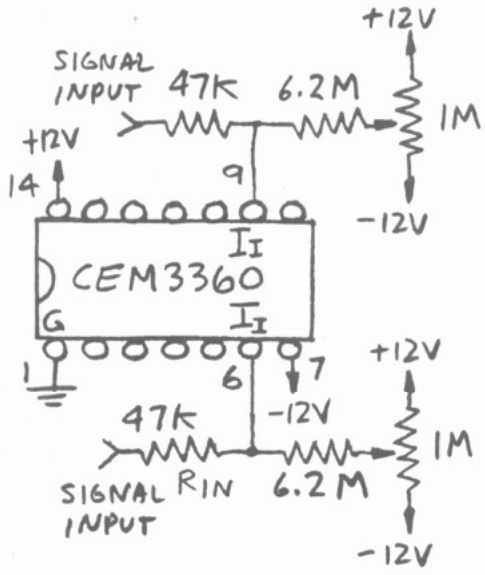


FIGURE 7: CONTROL FEEDTHROUGH TRIM

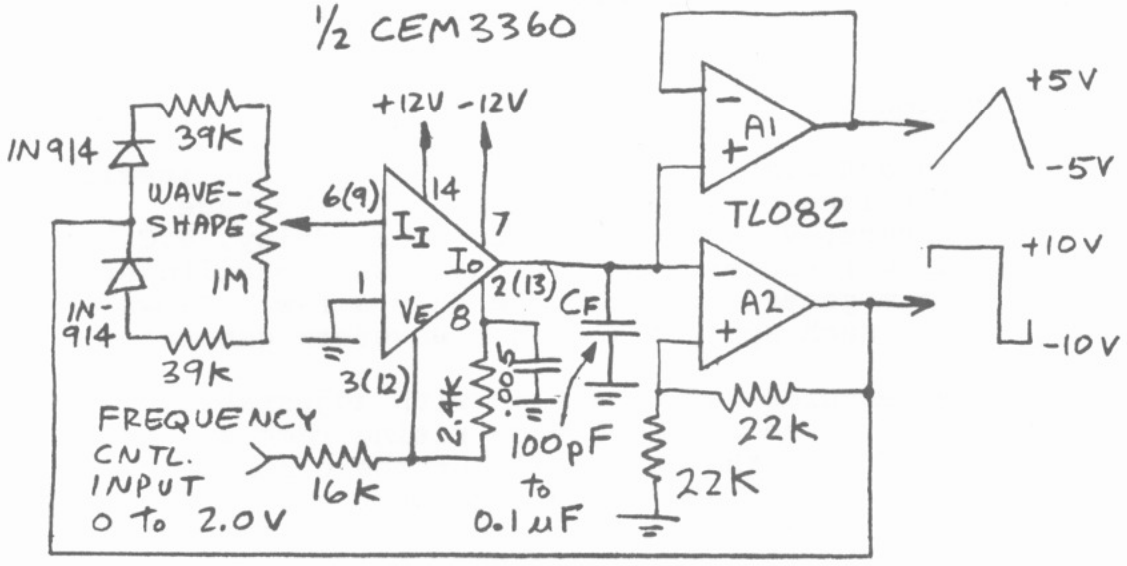


FIGURE 8: V.C. WAVEFORM GENERATOR

!)19AIP

CEM3372 uP CONTROLLABLE SIGNAL PROCESSOR Preliminary 8/27/82

General Description

The CEM3372 is a general purpose signal processing device for audio tone sources. Included on-chip are a two channel voltage controlled input mixer, a dedicated 4-pole low pass voltage controlled filter with voltage controllable resonance, and a quality final voltage controlled amplifier. With the exception of the filter cut-off frequency, all control inputs are very low bias current, high impedance inputs which range from 0 to +5 volts. This feature allows the common DAC output voltage in a microprocessor system to be multiplexed to these inputs with only a CMOS analog switch and hold capacitor, thus eliminating the usual Sample & Hold buffers.

The two input VCAs of the mixer feature audio taper control scales and high attenuation at zero contol voltage. The signal inputs are low level (80mV.P.P. for 5% THD), allowing multiple tone sources to be conveniently mixed into each channel.

The filter is the standard four pole low pass with Butterworth type response. Another VCA is provided to allow overall feedback, and hence amount of resonance, to be voltage controlled. A unique feature of this filter is that, unlike others of this type, the passband gain remains constant as the amount of resonance is varied, thus eliminating the annoyin drop in volume at higher resonance settings. Other features include wide frequency control range, temperature compensated transconductors, low noise, low control feedthrough, and a smooth behaviour when swept.

The final output VCA is a current in, current out type, allowing multiple inputs to be easily mixed into its input, and easy interface of its output to the rest of the system. The control scale is very linear, and the point at which the VCA shuts off is very well defined (+100mV ±50mV). Owing to its exceptionally low noise and exceptionally low control feedthrough without trimming, this VCA is well suited to being controlled by fast transient waveforms.

Features

- 2 channel V.C. input mixer, 4-pole low pass VCF, & quality final VCA all on one chip
- low external parts count
- low cost
- 0 to +5V, hi Z control inputs for Level A & B, Resonance, & Final Gain; interfaceable directly to CMOS multiplexer from DAC
- VCF uses open loop design for enhanced sound richness
- VCF has constant loudness as resonance changed
- temperature compensated VCF transconductors
- low level, non-inverting VCF frequency control input for easy mixing of control sources
- final VCA has low feedthrough without trimming

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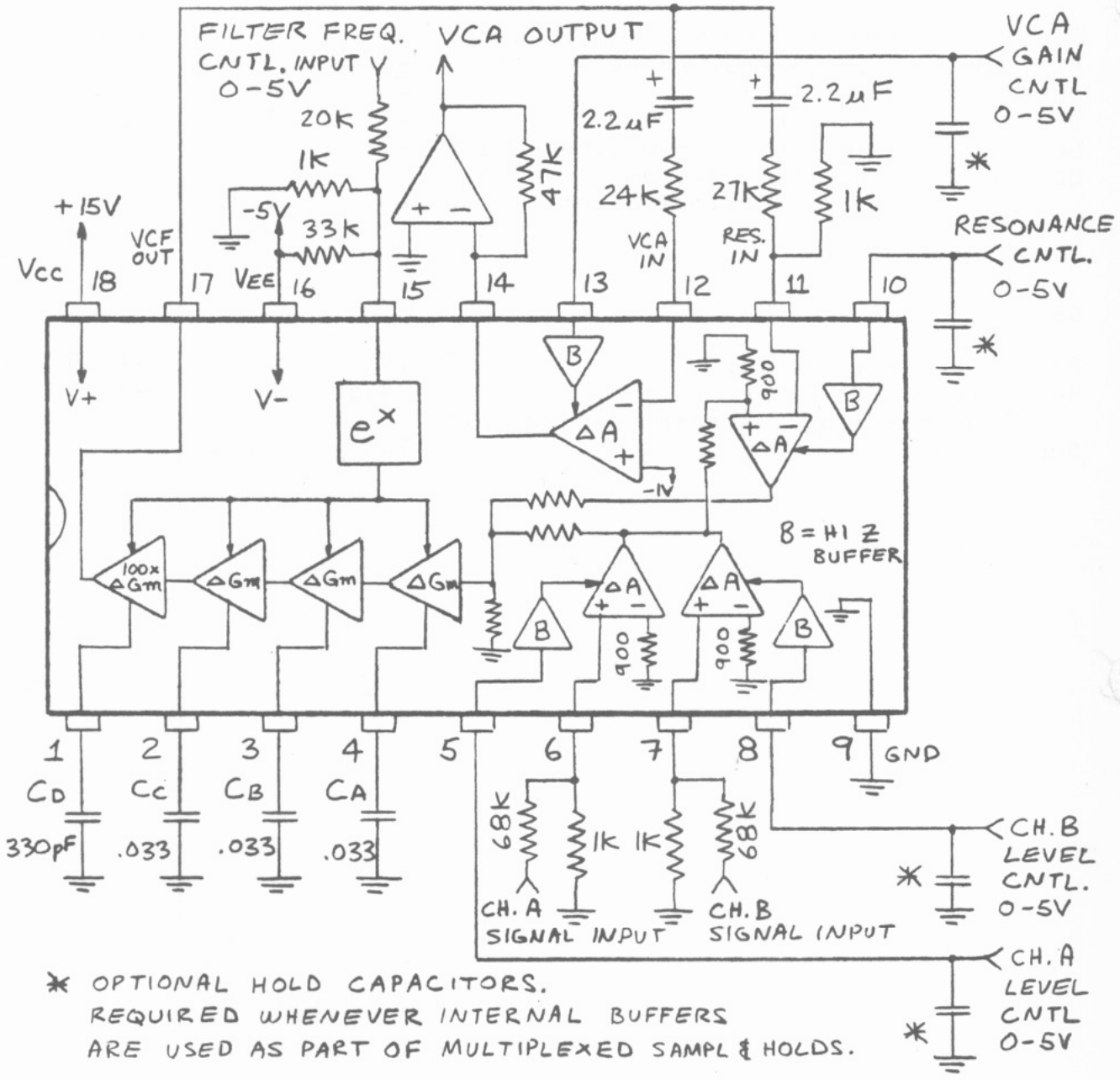
CEM3372 SPECIFICATIONS — Prliminary 8/27/82

Parameter	min.	typ.	max	units
Input VCAs				
Gain Range for 0-5V Control:	0-28.0	0-35.0	0-42.0	
Input Signal for 5% THD:	-	80	-	mV.P.P.
Attenuation at Vcntl=0:	80	100	120	dB
DC Control Feedthrough:	-	0.5	1.5	V
Control Input Bias:	0	+0.1	+0.5	nA/V
Gain Variation(unit to unit):		±2		dB
VCF				
Frequency Control Range:	14	-	-	octaves
Resonance Control Range:	Q=0.7	to oscillation		
Frequency Control Voltage for 14 octave range:		-150 to +100		mV
Frequency Control Scale:	+57	+60	+63	mV/decade
Initial Frequency at Vc=0: (Ca=Cb=Cc=0.03uF; Cd=300pF)	650	1000	1650	Hz
Frequency Control Input Bias:	-0.5	-1.2	-2.5	uA
Resonance Control Voltage required for oscillation:	+3.7	+4.2	+4.7	V
Resonance Control Input Bias Current:	0	+0.1	+0.5	nA/V
Resonance Input Signal Gain for 0-5V Control:	0-110	0-135	0-160	
Maximum Output Swing:	9	10	11	V.P.P.
Nominal Output Swing for 5% THD (resonance CV=0):	2.2	2.5	2.8	V.P.P.
Nominal Output Swing with Resonance:	4.4	5.0	5.6	V.P.P.
DC Output Shift Over 10 Octave Range (-120 < Vc < +60 mV):	-	100	250	mV.P.P.
Output Noise, Filter Wide Open:	-	-	200	uV.R.M.S.
Output Sink Current:	-0.5	-0.7	-0.9	mA
Output Source Drive Current:	-	-	+3.0	mA
FINAL VCA				
Gain Control Range:	100	120	-	dB
Maximum Signal Current Gain:	0.87	1.00	1.13	
Control Voltage for Maximum Gain:	4.25	5.00	5.75	V
Maximum Attenuation:	100	120	-	dB
Control Voltage for Maximum Attenuation:	+50	+100	+150	mV
Control Input Bias Current:	±0.1	±0.5	±3.0	nA/V
Voltage at Signal Input Summing Node:	-1.1	-1.0	-0.9	V
OPutput Voltage Compliance:	-0.2	-	Vcc-1	V

Maximum Recommended Signal Input Swing:	-	-	±200	uA	
Maximum Possible Signal Input Swing:	±0.5		±0.8	mA	
Output Noise:	-	-	1.0	nA	R.M.S.
THD at ±200uA input:	-	1.0	3.0	%	
DC Output Offset at Maximum Attenuation:	-	-	1.0	nA	
DC Output Shift from Maximum Attenuation to Maximum Gain:	-	0.05	0.5	uA	

GENERAL

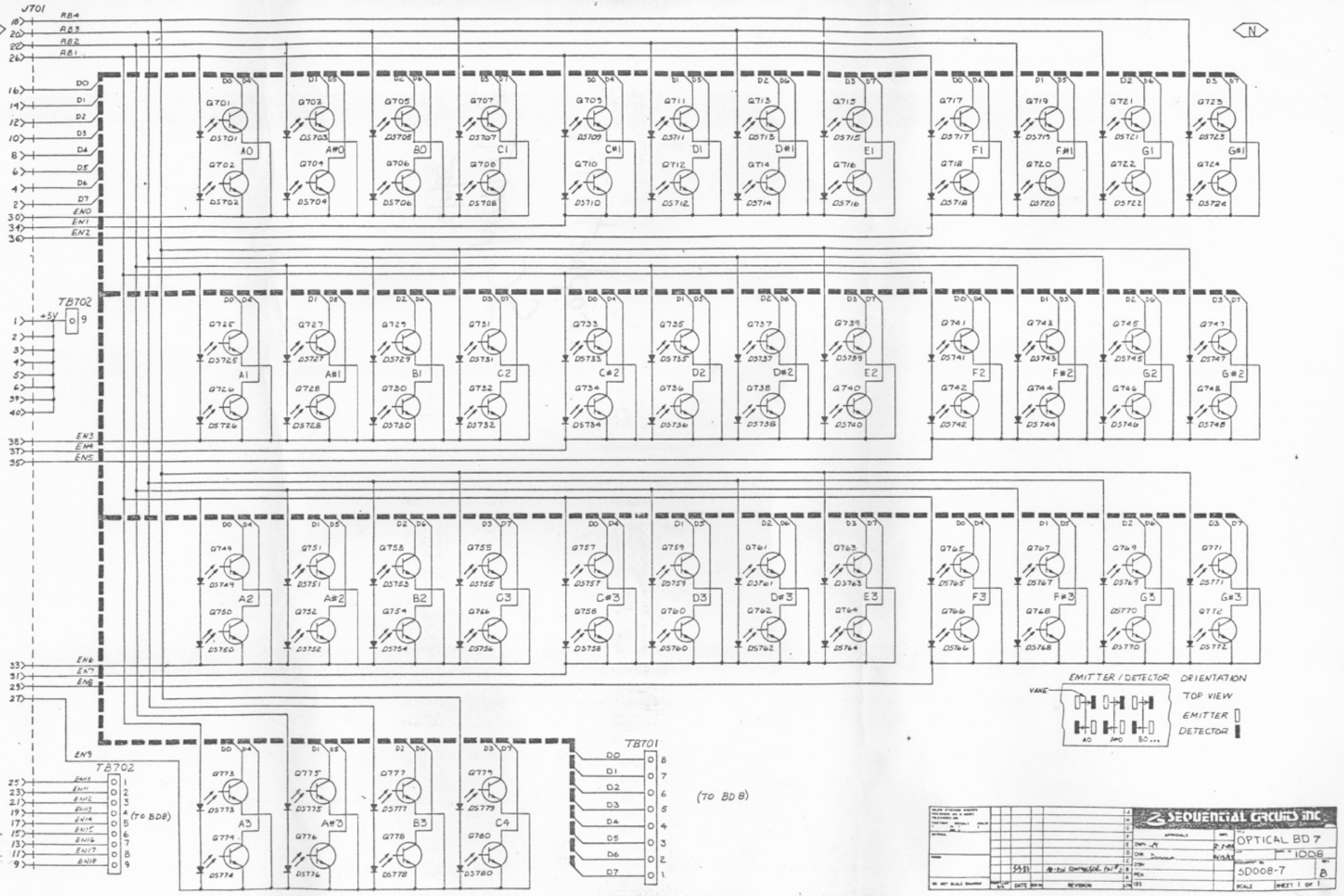
Positive Supply Range:	+9.5	-	+20.5	V
Negative Supply Range: (Maximum Supply Across Chip is 25V)	-4.5	-	-15.5	V
Supply Current:	7.0	9.0	11.0	mA



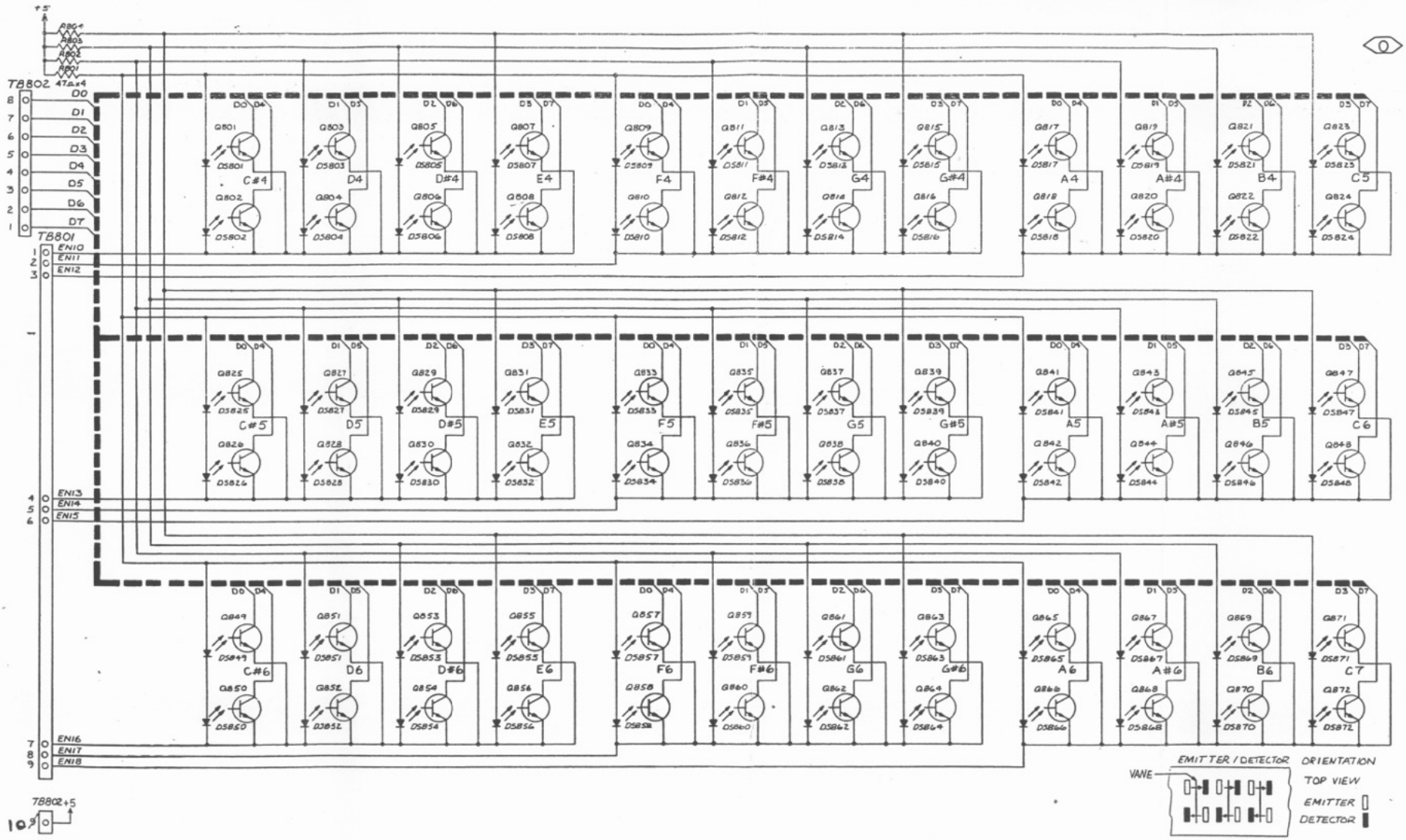
CEM3372 μP CONTROLLABLE SIGNAL PROCESSOR

BLOCK & EXTERNAL CONNECTION DIAGRAM

SCHEMATIC N
SD008-7 1/1
(PCB 7)
50% reduction
11 x 17
Black Line


J701
TB702
TB701
TB702
(TO BD8)
(TO BD 8)
EMITTER / DETECTOR ORIENTATION
VANE
TOP VIEW
EMITTER
DETECTOR
SEQUENTIAL CIRCUITS INC
OPTICAL BD 7
5D008-7
8

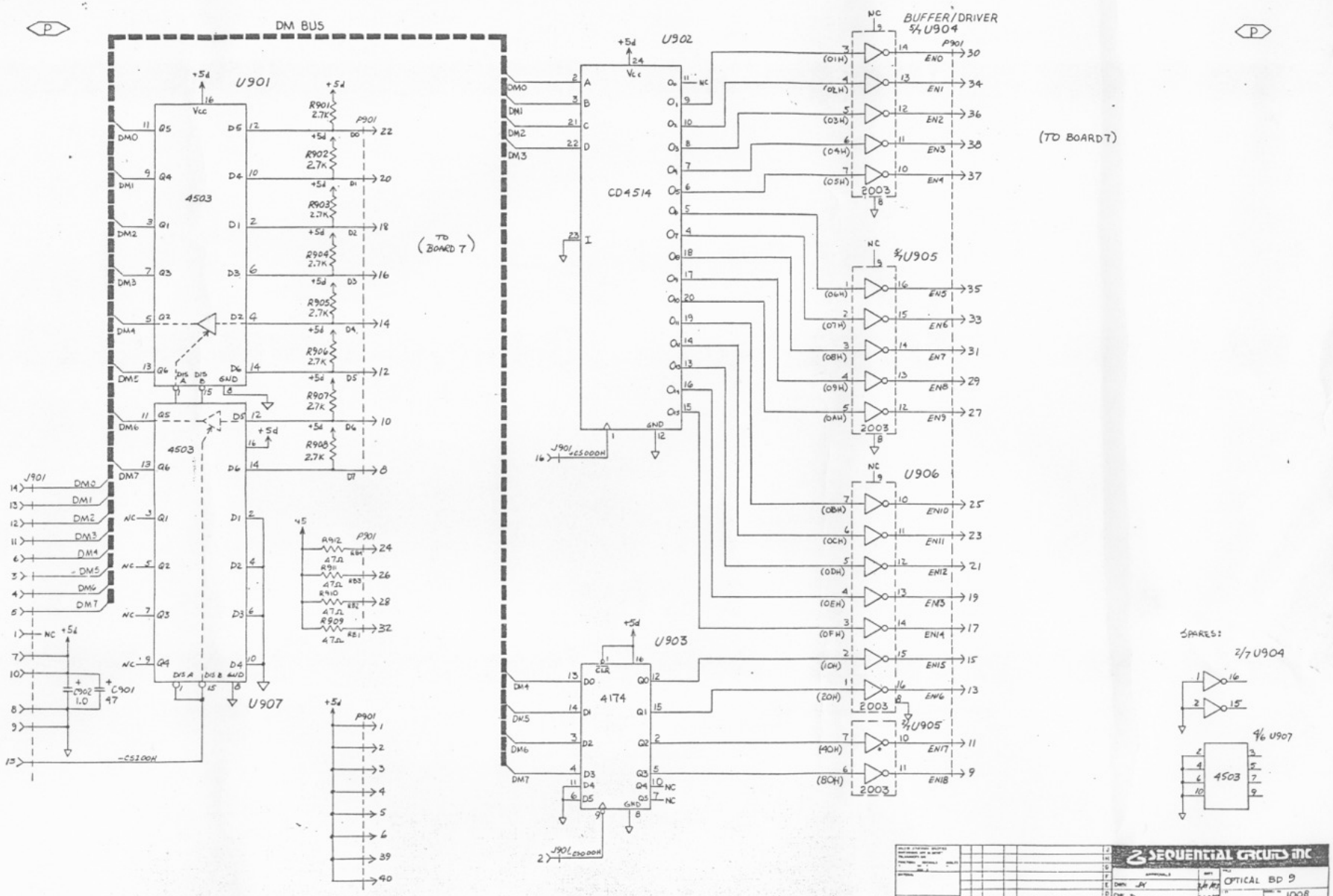
SCHEMATIC O
SD008-8 1/1
(PCB 8)
50% reduction
11 x 17
Black line



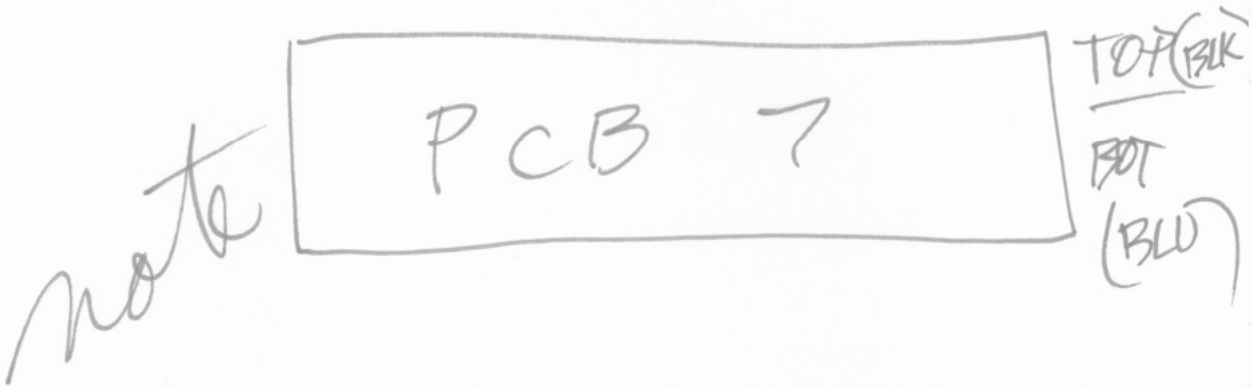
SD008-8

SEQUENTIAL CIRCUITS INC			
DRN JV	2-3-83	TITLE: OPTICAL BD8	
CHK		SIZE: A	DWG. NO. 1008
DES		DOCUMENT NO. SD008-8	REV A
PCH		SCALE	SHEET 1 OF 1
ISS			

SCHEMATIC P
SD008-9 1/1
(PCB 9)
50% reduction
11 x 17
Black Line


DM BUS
U901
4503
U907
U902
CD4514
BUFFER/DRIVER
5/U904
5/U905
U906
U903
4174
2003
(TO BOARD 7)
(TO BOARD7)
SPARES:
2/7 U904
9/6 U907
SEQUENTIAL CIRCUITS INC
OPTICAL BD 9
SD006-9
B

PCB 7 DESIG MAP
PP008-7
PCB 8 DESIG MAP
PP008-8
1:1
11 x 25 (?)
2 color
Top layer black line/black screen
Bottom layer Blue screen



PCB 9 DESIG MAP
PP008-8, 9
50% reduction
11 x 17
Black line

7-9.1 PRECAUTIONS

The optical system will respond to ambient light. While servicing, it should be shielded to avoid spurious indications.

The optical devices (infrared LED and phototransistor) are very fragile. Do not bend the leads as this may cause an invisible failure.

As mentioned in the Keyboard section, the mounting of PCBs 7 and 8 to the keyboard back rail is critical. When removing them, note exactly how the shims are arranged, and when reassembling, restore them exactly as found.

Do not strain the flexible jumpers between PCBs 7 and 8.

7-9.2 DEAD KEYS

The functional test for the optics was given in the Keyboard section (see page K.3). Perhaps that test has revealed some dead keys.

Dead keys can be caused by a failure of any of the four sensor parts per key. If the upper emitter or detector is open, it will look to the computer as if the vane has never moved past the 30% point. So the note will not turn on. If the upper sensing pair is OK but one of the lower pair is open, it will look like the vane has never arrived at the 70% point. The computer will interpret this as a velocity of 0, and therefore not turn the note on.

Sometimes a cold solder joint at the emitter of the lower detector (not to be confused with the photo emitter itself) will prevent the EN line from reaching the next set of key optics, causing another key to appear to be dead. A quick "touch-up" of the solder points of the neighboring optic sensors may cure the dead key, and is recommended before replacing any parts.

It is best to use the diagnostics described in this section to test the optical system. But if a diagnostic EPROM (DT8_4) is not available there is an easy way to test the detectors. Connect a voltmeter to the collector of each detector (see Figure 7-9.2). With the vane at rest the meter should read about +5V. Now shine a penlight at the detector. If the detector is good, the meter will read a "low," near 0V. If both detectors are good, one of the emitters must be bad. As the emitters are in series, rather than try to deduce which of the two is faulty, it may be easiest to replace one at random, then check to see if the other needs to be replaced.

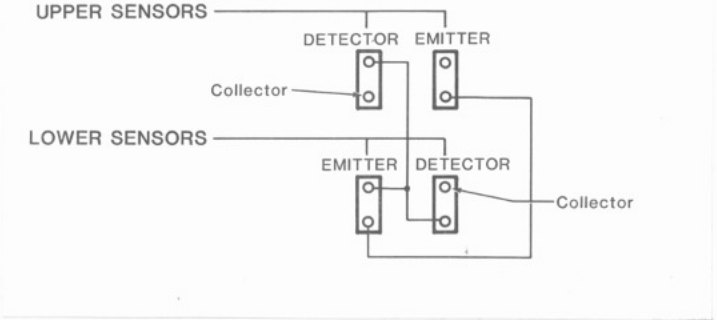


Figure 7-9.2
DETAIL OF OPTICS BOARD, BACK VIEW (SOLDER SIDE)

7-9.3 OPTICAL SENSOR DIAGNOSTICS

The Optics PCBs are part of the Main (Z-80) computer system. The optical sensor diagnostics are contained in the special "DT8_4" EPROM which is required to test the Z-80 system (order SCI #Z-1017.)

1. Switch power off.

2. Remove the top panel (see page O.20).

3. From PCB 3 (at the left) remove U322, MAIN ROM. (Observe cautions discussed on page 3.14)

4. Orient DT8_4 EPROM correctly, with end notch facing left, and install.

5. If Z-80 was disabled for Z-8002 test, unground the Z-80 BREQ test point. (Ignore this step if you have not yet run Z-8002 diagnostics.)

6. Disable Z-8002 by clipping the Final BREQ test point (located just above U348) to ground. There is a GND test point in the middle of the board.

7. Switch power on. The control panel will not light. The Main system is waiting for a bank of diagnostics to be selected. There are two banks of tests in the DT8_4 EPROM:

	Page
Bank 1 = MAIN computer system diagnostics	
M1 I/O Test	3.16
M2 LED Test	1/2.11
M3 Local RAM Test	3.17
M4 Common RAM Test	3.17
M5 ADC Test (pots, pressure sensors, wheels)	1/2.11, 10-14.7
Bank 2 = KEYBOARD tests for calibration and debugging	
K1 Optics (unmounted), looped scan test	7-9.11
K2 Optics (mounted), single step scan test	7-9.10
K3 Looped scan of pressure sensors	10-14.8
K4 Single step test of pressure sensors	10-14.9
K5 Optics (mounted), looped scan test	7-9.9
K6 Pressure sensor slope analyzer test	10-14.10

8. Main is selected at first. After this, to select a MAIN test, you must first press the LEFT program switch, selecting Test Bank 1. The The LEFT and RIGHT displays will read "(blank) 1" and "1 1" respectively for four seconds. The displays will then go blank. Pressing PROG/SEQ switches 1-5 will then select MAIN tests M1-M5.

9. To select one of the KEYBOARD tests, you must first press the RIGHT program switch, selecting Test Bank 2. The LEFT and RIGHT displays will read "(blank) 2" and "2 2" respectively. The displays will then go blank. Pressing PROG/SEQ switches 1-6 will select KEYBOARD tests K1-K6.

10. The following tests are related to the optical system: K1, K2, and K5. (Instructions for each test follow in this section.)

11. When done testing the optical system, you can perform the Main computer or pressure sensor tests (listed above), or perform the Final computer diagnostics (see page 3.19), or return to normal operation.

12. When all diagnostics are concluded, to resume normal operation:

a. Switch power off and install the operating PROM.

b. Remove BREQ ground from Z-8002.

c. Switch power on. (If the Main Common Ram test was run, no programs will be heard because they have been erased. A-440 won't be heard because PROG VOLUME has been set to 0 in the Scratchpad.)

d. Reinitialize the PITCH wheel (see page 1/2.6).

e. Reload programs (and sequences) through the cassette interface.

f. Because the test clears the Scratchpad, you must select both a program on the LEFT side and one on the RIGHT side. (This fills the Scratchpad from the Program memory.)

7-9.3.1 K5 OPTICS (MOUNTED), LOOPED SCAN DIAGNOSTIC TEST

See the setup instructions for this test on page 7-9.7.

1. Press 5. Only the 5 will be lit.

2. Press any key. If the upper velocity sensor is working and being read, the RIGHT LED will go on and the key number will be in the RIGHT display. If the lower sensor is working, the LEFT LED will light near the end of travel.

If no keys are being held but the RIGHT LED lights and a key number appears, check the vane height adjustment for that key. (See page K.7)

When the key is at rest, both the LEFT and RIGHT LEDs must remain off. If the LEFT LED is on, check the vane height, as well. (If this key condition is present in a machine with normal operating software, all four keys in that key's group will be disabled.)

7-9.3.2 K2 OPTICS (MOUNTED), SINGLE STEP SCAN DIAGNOSTIC TEST

See the setup instructions for this test on page 7-9.7.

Press 2.

This test indicates similarly to K5, except only one key is read at a time, starting with the lowest key. The current key number is shown in the RIGHT display. To advance key numbers, press 8.

While this test reads only one key at a time, each key is part of a four-key group which is strobed at once. You can use this test to isolate the faulty set (upper or lower) for a key. You can connect your scope either to the collector of one of the detectors (see page 7-9.4), or probe the data lines D0-D7 on the input side to the buss driver. (The schematic tells you which data lines to probe.) Of these two techniques, probing the data lines is easier because the lines are easily found on PCB 9 where there are the pull-up resistors.

7-9.3.3 K1 OPTICS (UNMOUNTED), LOOPED SCAN DIAGNOSTIC TEST

For test setup instructions, see page 7-9.7.

This test should only be used when the optical board is unmounted. To prevent false test indications, the optical boards must be shielded from ambient light.

Press 1.

Note: The number in the RIGHT display indicates the optics pair number, not the note number.

The test sequentially scans the keyboard from the bottom up. It checks each detector for a low on its collector. If the low is not read, the test stops and displays the designator number (as shown on the schematic) for that pair. For example, if the bottom sensor for the lowest key were faulty, the display would read 07 02. After noting this number you would continue the test by pressing 8. If a new fault is detected, the scan will again stop and display the designator number of the faulty pair. If no new fault is detected, then the scan will loop around to the original fault. If no faults are detected, the scan will loop endlessly and the displays will remain blank.

If there are multiple failures, after noting the designator numbers involved, you should examine the schematic for logical relationships between the devices which may point to a common problem.

This test allows you to find opens which cause emitters to fail to light or detectors to fail to pull down the driver input. The emitter is more likely to be failed. To confirm, shine a penlight at the detector and repeat the test. A successful test proves the detector works.

This test cannot find shorted data lines between collectors, nor shorted enable lines. The only exception here are shorts to +5V. (The "ground" plane of boards 7 and 8 is actually at a +5V potential). Shorts of this type will not allow enable or data lines to go low, thus they will be displayed in K1 as faults.

While the system is unmounted, select test K2. Key number 01 is displayed in the RIGHT display, and both the LEFT and RIGHT LEDs are on, because there is nothing blocking the sensors. If the RIGHT is off, shine a penlight at the upper detector. If it goes on, then the upper emitter is bad. Likewise for the LEFT LED and lower sensor.

Using a spare vane (or other infrared-opaque material), block both sensors. Both LEDs should go off. If one or both of the LEDs stay on, then it is likely that the data line (or lines, if both are on) is shorted to other data lines of detectors in that group. To find out exactly which lines the short may be to, keep the sensors blocked while blocking each of the other three keys. When the shorted detectors are found, the LEDs will go off. This will at least tell you which data lines are shorted, though you will have to power down and use your ohmmeter and eyes to find the exact location of the short.

After checking key #1 fully, advance to check the second, third and fourth keys in the group by pressing PROGRAM/SEQUENCE 8. It need be done on only a single group of 4 to check all 8 data lines on the system.

If all sensors are blocked and the LEDs don't go off, then it is likely that the Enable line for that group is shorted to another Enable line. This short turns on a second group of four keys which override the set being blocked. To find the short, block adjacent groups of four keys.

There is a final way to use test K2 to confirm there are no shorted enable lines on an unmounted optical system. Select key 01 and block it. If both LEDs go off, advance to key 05 and repeat. Continue with the first keys in each group of four (09, 13, 17...). Should you find a key that doesn't turn off the LEDs when blocked, simultaneously block the first keys of adjacent groups to find the shorted enable line.

7-9.4 PCB 9 ACCESS

To remove PCB 9 (optics control board), it should be possible to unscrew the board from PCB 7 without removing the keyboard.

7-9.5 PCB 7 AND 8 REMOVAL

CAUTION! The mounting of these two optics boards is crucial to the performance of the machine. When remounting these boards it is very difficult to restore proper alignment, without further adjustments of the keys (as described in the Keyboard section). Also, the wooden mounting screw holes are weakened with each operation. Therefore do not remove these boards unless it is absolutely necessary.

1. To remove these two boards, the keyboard must be removed (see page K.11). While hex heads are provided for the mounting screws, it is not likely that the boards can be easily removed and accurately remounted while the keyboard is still mounted in the chassis.

2. Unmount PCB 9 from PCB 7.

3. Remove mounting screws along bottom edge of boards. Make careful note of placement of shims between the boards and the keyboard.

4. If only PCB 7 or 8 is unmounted, do not stress the interconnecting jumper.

5. Inspect hammer foam. Replace if necessary. (See Keyboard Action drawing, page K.1).

6.When remounting the optical boards, be especially careful to not strip the mounting screws.

7. After remounting the optical boards, check the height of the key vanes (see page K.7).

7-9.6 EMITTER OR DETECTOR REPLACEMENT

It is possible to replace optical devices while the keyboard is mounted in the chassis, but working space is very tight. Whether success can be expected depends on the exact location of the device, your tools, and technique. In the general case, it may be easier to first remove the keyboard:

1. Remove the keyboard. (For instructions, see K.11).

2. Only if absolutely necessary, unmount PCB 7 or 8 from the back rail as required, and support the board to minimize stress on the jumper ribbon to the other board.

3. With small wire cutters, split the body of the device between the leads.

4. Desolder each lead with a low-power (25W) iron.

5. Use a "solder-sucker" to clean the holes.

6. An optical sensor lens (seen as a small circle on one side of the sensor) should face in, toward the other half of the sensing pair. Recently, sensors have paint on the back (white on emitters, black on detectors). Earlier sensors have paint on top. If one of the emitters is installed backwards, neither the upper or lower sensor of a key will work. Sensor pairs have "stops" to prevent the part from being mounted too close to the PCB.

7. Heatsink leads of new device, solder, and trim leads.

7-9.7 PCB 7 AND 8 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-276	PCB 7 ASSEMBLED
DS701-80	Optical Emitter	L-007	MOTOROLA MLED 71
	RB1-4 are a current-limited power supply for the infrared LEDs. The -EN signals are decoded on PCB 9. They sequentially select each of the ten groups of eight sensors (four keys) on PCB 7, and nine groups on PCB 8. When the -EN strobe goes low, all the emitters in that sensor group light. For optimum optical transfer ratio, LED string current is 35 mA.		
J701	Two used for 40 pins	J-065	20-PIN DBL ROW SKT
	This is the sole connection to PCB 9. In Rev A this had 34 pins.		
Q701-80	Optical Detector	T-014	PHOTO TRANS MRD701
	D0-7 are data lines from the optics boards, which are read by an input port on PCB 9. The sensor group is activated by the -EN signal. As long as the vane stands between the LED source and phototransistors Q701/2, the collectors will be high (as they are pulled up by R901 and R905 on the Driver inputs.) But as they key is pressed, first Q701 then Q702 turn on, allowing the -EN0 strobe to pull D0, then D4 low.		
TB701	Jumper to PCB 8	E-134	1-1/2" 9-PIN JUMPER
TB702	Connects PCB 8 to 7	E-133	1-1/4" 9-PIN JUMPER
		PC008-7B	LEFT OPTICAL BOARD
			Rev B incorporates oval mounting holes.
		Z-277	PCB 8 ASSEMBLED
DS801-72		L-007	MOTOROLA MLED 71
	Same as DS701-80 with -EN strobes coming from PCB9 via PCB 7 .		
Q801-72		T-014	PHOTO TRANS MRD701
R801-04		R-043	47
	Supply current limited +5V to optical emitters DS801-72.		
		PC008-8B	RIGHT OPTICAL BOARD
			Rev B incorporated oval mounting holes.
	Hold PCBs 7 and 8 to back rail (9 used)	M-430	6-32 x 3/4" HEX HEAD SMS

7-9.8 PCB 9 HARDWARE DESCRIPTION

DESIGNATOR	FUNCTION	SCI PART #	PART DESCRIPTION
		Z-278	PCB 9 ASSEMBLED
U901	Optics Input Port	I-216	4503 HEX TRI-STATE BUFFER
	U901 drives the lower six bits of keyboard data on to the Main Data Buss. R901-08 ensure that the keyboard data lines from the sensor collectors float high. When -CSI00H is high, the driver output is high-impedance so the Data Buss is not affected. When the computer enables a group of eight sensors, the data for blocked sensors will be high while unblocked sensors will produce a low on D0-8. -CSI00H then goes low, placing this data on the buss, from where it is retrieved by the CPU.		
U902	Optics Strobe Decoder	I-218	4514 4-16 DEMUX
	When +CSO00H returns low, a four-bit binary number on the A, B, C, and D inputs is decoded to one high output. This chip selects one of fifteen sensor groups. (Pin 23 must be grounded otherwise all outputs will be forced low.)		
U903	Strobe Latch	I-228	4174 HEX LATCH
	When -CSO00H returns high, U903 latches four more bits used to select the remaining sensor groups.		
U904-06	Optics Drivers	I-235	MC1413 (2003)
	The nineteen strobe signals are inverted and buffered by the 2003s. -EN0 through -EN9 select PCB 7 optic groups. -EN10 through -EN18 go to PCB 8 (via PCB7), where they operate the Right optics.		
U907	Optics Input Port	I-216	4503 HEX TRI-STATE BUFFER
	Drives the most significant two bits of keyboard data on to the Main Data buss, similarly to U901.		
C901		C-055	47 35V ELECT AXIAL
C902		C-020	1.0 25V 20% TANT RADIAL
J901		J-007	16-PIN DIP SOCKET
P901	Two used	P-043	20-PIN HEADER
	In Rev B, pins 6 and 7 must be tied together (otherwise the top half of the keyboard won't work).		
R901-08		R-035	2.7K
R909-12		R-043	47
	R909-12 provide current-limited +5V, RB1-4, to the LEDs on PCB 7.		
		PC008-9B	OPTICS DRIVER BOARD
	For U902.	J-017	24-PIN DIP SOCKET
	Holds PCB 9 to PCB 7 (2).	M-421	6-32 x 7/16" STANDOFF
	Holds PCB 9 to M-421 standoff (2).	M-431	6-32 x ¼" ALN HD CAP SCREW

1008/4 FINAL 3_3 improves filter tuning.

1008/36 MAIN/FINAL 3_4:
Eliminates pop when tune is pressed.
Eliminates spurious notes when leaving tune.
OSC B FREQ is correctly initialized when switching off LO switch.
MOD wheel initialized to actual position.

1008/38 The 8253 used must be a special, "tight-spec" version. Order SCI #I-414.

1008/82 DT8_4 Main Computer diagnostics released. Contains two banks of tests:

Pressing LEFT lights three 1s for four seconds. When they go out, press PROGRAM/SEQUENCE switch for desired test:

1	I/O Test
2	LED test
3	RAM test
4	Common RAM test
5	ADC test

Pressing RIGHT lights three 2s for four seconds. When they go out, press PROGRAM/SEQUENCE switch for desired test:

1	Optics, unmounted
2	Optics, mounted
3	Pressure, Looped scan (threshold calibration)
4	Pressure, single-step scan (threshold calib.)
5	Optics, mounted, looped
6	Pressure, slop analyzer

Detailed instructions are in forthcoming TM1008.

1008/87 Model 866/Main 3_5, Final 3_5. Service Center cost is $75. Customer cost is $100 + installation.
Adds MIDI clocking of sequencer.
Adds MID channel select.
Fixes running status byte problem.
Changes SECOND RELEASE to match Roland and Yamaha.

1008/94 MAIN 3_6 released. This fixes Mono mode operation. In previous levels, reception of MIDI pressure information for one key in Mono mode would permanently disable pressure information for that key from the -T8s keyboard.

1008/ FINAL 3_6 released. Fixes a problem with the release velocity function.

-T8 Tech

Tech Manual

TN1008-0	Preliminary Service Data
TN1008-3	Diagnostic Procedures (not included in TN1008-0)
TN1008-4	How to Replace the Prophet-T8 Firmware (Cost: $0.22)

See FB12 Software, DT8_4

T-8 Optic board Mounting Procedure

SCOPE: This procedure is to be used when installing the optic board support brackets.

REQ'D. Hardware:

4 - 8-32 x 3/8" BLK Pan Head Phil. M.S. (P/N M-403)
5 - 8-32 Hex Nuts (P/N M-091)
5 - #8 INTERNAL TOOTH STAR WASHERS (P/N M-191)
1 - 8-32 x 3/8" BLK FLAT HEAD C.S. PHIL. M.S. (P/N M-418)
1 - MW1008-13 RIGHT SUPPORT BRACKET
1 - MW1008-14 LEFT SUPPORT BRACKET
1 - ROLL - Adhesive tape 3/4" WIDE (doublkback)
1 - Strip - 24" x 3/4" 15 MIL Thick Nylon
1 - 1/4" SOCKET & RATCHET
1 - 1/4" OPEN END WRENCH.
1 - 5/32 x 6" Lg high SPEED DRILL
1 - Power DRILL
1 - Center punch
1 - Phillips head SCREW DRIVER
1 - Metal Countersink DRILL
1 - Exacto KNIFE
1 - 11/32" Nut DRIVER.

PROCEDURE:

1) Using a 1/4" RATCHET and/or 1/4" OPEN END WRENCH Remove the 5 - M-430's USED to attach the optic boards to the back RAIL

2) USING THE EXACTO KNIFE, CUT THE MYLAR and attach it to the undersides & the sides contacting the optic boards of both brackets. TRIM all holes & edges.

3) Sandwich Optic board #7 between the back rail & support bracket # MW-1008-13.

4) Sandwich Optic board #8 between the back rail & the support bracket #MW1008-14.

5) Using the optic board mounting holes and the support bracket slots, align the mounting holes & slots and REINSTALL the 5 - M-430's.

6) With bracket securely mounted to the optic boards & back rail, locate one position for each slot of the brackets facing the bottom panel. Center punch each location.

7) Being careful not to damage the optic boards, drill one hole through the bottom panel, for each slot.

8) With the keyboard in the position to be played directly in front of you, countersink the hole 2nd from the Right.

9) Vacuum ~~machine~~ T-8 to remove all loose metal particles.

10) In all but the hole just countersunk, install 4-M-403's. from the bottom side. & M-91's & M-191's from the inside.
Tighten screws with the Phillips head screw driver and the "/32" Nut driver.

11) In hole countersunk hole, install 1-M-418 from the bottom & 1-M-91 & M-191 from the top. Tighten with Phillips screwdriver & 11/32 Nut driver.

12) Check to insure all screws are tight

13) Check Jags. Some repositioning may be required.

KEYBOARD ACTION DWG and PARTS ID
SK 1-25-84
50% reduction
(11 x 17)

~~Only source~~ necessary - only source

- Spring Part #s

K.1 KEYBOARD ACTION FUNCTIONAL TEST

Note: This section covers basic keyboard function and mechanical adjustments. For data regarding the optical system, see section 7-9. For the pressure system, see section 10-14.

Note: Be careful not to scratch the keys. Replacement of key caps is a time consuming process and well worth avoiding. As the -T8 keyboard is made from one piece of wood it is not possible to simply replace a key.

Select the basic program (see page 4/5.9).

The keys themselves should never be touched with harsh chemical cleaners. As with acoustic pianos, the keys are best cleaned by light rubbing only with a slightly dampened cloth. Don't rub hard--use mild soap only if necessary.

First note the cosmetic flaws. It is inevitable that someone will ask to have a key top replaced because of a cigarette burn or some such. Replacement can be handled by using standard piano techniques (see page K.10).

1. Check the level of the keys by looking along the edge. Don't forget the black keys, too. If necessary, identify errant keys with a small piece of masking tape (or other low-tack tape such as drafting tape) placed on the rear surface of the key. Shims and excessively worn support washers (see page K.1) can be replaced when the case is opened.

2. Play a chromatic scale over the full keyboard to check that every key at least produces sound.

3. Turn off all audio and listen carefully to the keys themselves as you again play up from the bottom. Slowly "trill" adjacent keys to reveal rubbing or sticking. Hold down each black key and check that this doesn't cause the adjacent white ones to stick. Listen too for rubbing or scraping from inside the chassis. This may indicate a damaged velocity vane. Or since the vanes don't bend themselves, such noise may indicate warping of the keyboard. When exposed to high humidity, the wooden keyboard may eventually absorb moisture and expand. The way this has tended to occur is that the back rail tends to lift up, which tilts the two Optical boards towards the vanes, reducing the clearance and in some cases actually pushing the PCBs against the vanes. The Optical boards themselves have also been known to warp. To correct any warpage, or tendency to warp, install the Optical board support brackets, if not already installed (see page K.12). If only a few notes are affected, it may be more expedient to reposition the vane forward on the hammer, after trimming the front (straight) edge of the vane.

Warpage also sometimes causes the hammers to hit the inside top rail. This must be corrected through the vane height adjustment (see page K.7).

Besides changing the weather, only disassembling the keyboard and patiently sanding the key edges can correct friction between adjacent keys.

It is not recommended that you try to bake the moisture out of a warped keyboard, as inexperience with seasoning techniques may permanently ruin the keyboard. The wood will eventually stabilize to its environment, although minor adjustments may be needed periodically.

K.1.1 KEYBOARD MODES FUNCTIONAL TEST

1. With PRESET on, switch SINGLE on (if it is not already on).

2. Play the keyboard to check that the same program plays across the whole keyboard.

   It should be possible to play and hear up to eight different keys.

3. Hold the key to be the lowest key on the right side, and press SPLIT.

4. Check that different programs are played on the left and right.

   It will be possible to play up to four voices simultaneously on each side.

5. Switch to DOUBLE mode and check two programs are played at once.

   Only up to four keys (maximum) can be held at once.

K.1.2 VELOCITY RESPONSE FUNCTIONAL TEST

1. Switch PRESET on and select a suitable velocity program, such as Factory R11 (Piano) or R15 (Vibalimba).

2. Play all keys, first forcefully, then slowly, and listen for consistency of response from key-to-key.

3. Identify any malfunctioning keys (with tape or such).

   Note: The four VELOCITY SENSITIVITY controls are tested in conjunction with the envelope generators (see page 4/5.29/30).

K.1.3 PRESSURE RESPONSE FUNCTIONAL TEST

Every key must be checked for proper pressure response. This is done by applying the pressure signal to bend oscilllator frequency, and listening for smooth and consistent pitch bending.

1. Select the basic program (see page 4/5.9).

2. Switch PRESSURE-MOD FREQ A on.

3. Switch A-440 on.

3. Hold the lowest key (A0), and tune OSCILLATOR A FREQUENCY to the A at approximately 5½ on the dial.

4. Switch A-440 off.

5. Starting at the bottom, check that for each key:

   a. There is a threshold between the bottom of key travel (when played with normal velocity), and the actual engagement of the pressure sensor. In other words, with the key down but no more force applied than needed, there should be no pitch offset. (For threshold adjustment, see page K.8.)

   b. No key acts as a pressure "switch."

   c. Pressure bends each key by at least an octave, without needing excessive force.

   d. There are no jumps greater than a major third (three semitones) in the bending. To hear the jumps, you have to bend the note slowly.

6. When you get up to the center of the keyboard, return OSC A FREQUENCY to 0.

7. Identify any malfunctioning keys (with tape or such). You'll need to note somehow whether the key has a threshold problem or a jumpy sensor.

   Note: The PRESSURE-MOD controls are tested in conjunction with the modulation system (see page 4/5.26-28).

K.1.4 GLIDE/UNISON FUNCTIONAL TEST

1. Select the basic program (see page 4/5.9).
2. Check that SINGLE is on.
3. Play a cluster of eight keys in the center of the keyboard.
4. Turn GLIDE to 10.
5. Now, at the same time, play four keys at the bottom and four at the top.

   This demonstrates polyphonic glide.

6. Switch UNISON/TRACK on.
7. Hold one key at the top of the keyboard.

   After all voices have glided up to this new key, the keyboard will operate in unison (all voices assigned to one key).

8. Turn GLIDE to 5.
9. Play the lowest and highest keys, to demonstrate medium-rate glide.
10. Turn GLIDE to 0.

K.1.5 TRACK FUNCTIONAL TEST

1. Switch UNISON/TRACK off.
2. Hold a chord with one hand, and press UNISON/TRACK.
3. Release your hand, then play single keys.

   This demonstrates chord tracking.

4. Switch UNISON/TRACK off.
5. Connect footswitch to UNISON/TRACK FOOTSWITCH jack.
6. Hold a chord.
7. Press UNISON/TRACK footswitch.
8. Check that chord tracks keyboard.

K.2 KEYBOARD SERVICE--PRECAUTIONS

The following procedures cover alignment of the keyboard action only. Please also consult section 7/8/9 for velocity sensor diagnostics, and section 10-14 for pressure sensor diagnostics.

The keyboard is massive enough to absorb the velocity and pressure forces. However, like all wooden instruments, the keyboard is subject to the weaknesses of wooden parts: off-center holes, drifting holes, and warping. Therefore periodic rework may be needed also to renew felt or foam. But keep in mind that in a mechanical system of this complexity, there will always be some imperfection. Constant, neurotic tweaking will wear everything down and guarantee poor performance. If it works, don't mess with it.

Many of the keyboard parts are standard items available from piano supply houses. However, it is not an easy or trivial matter to overhaul the -T8's keyboard. At this time of writing, we are recommending that you send keyboards in need of extensive work back to the factory.

NOTE: The procedures given below are in order of complexity, with the simplest (and usually commonest) given first. Any necessary repairs or replacements should be undertaken before making fine adjustments.

K.2.1 KEYBOARD LEVELING PROCEDURE

See Keyboard Action Drawing, page K.1.

Look along the keyboard edge for unevenness of height. Don't forget the black keys. Measure heights of white keys by sliding a thin ruler between two keys near the front. The tops of white keys should be about 2.2" from the bottom panel. Wear usually shows up in the middle of the keyboard. Identify the bad keys with tape.

After removing the control panel (see page 1/2.12), remove the misaligned keys from the keybed. To remove a key, raise the hammer then lift the key off of its balance pin. Visually inspect the rest foam. Compare the resting height of the back of the keys.

Most key height problems can be solved by changing the number of paper shims under the balance punching. For each bad key, remove the present balance punching and shims. Place a new balance punching over the pin. Place original combination of white and blue shims over the punching. (Original shims may usually be used again.) Place the key back in and check the alignment. When replacing a key, lift the hammer so that the felt "pedestal" area is not damaged by being forced against the capstan. Tweak the alignment by adding shims to raise the resting point, or removing them to lower it. If shims are not readily available, it may be necessary to improvise (using a small piece of paper). As no two keys are identical, there is no "correct" combination of white and blue shims. After selecting the shims, place the shims <u>below</u> the punching.

The only other factor affecting key height is the rest foam tape, which if worn, may cause the front of a key to be too high. Replacing the rest foam tape involves removing all keys and is usually not necessary as the foam will not wear down easily.

K.2.2 VANE REST HEIGHT ADJUSTMENT

This adjustment follows keyboard leveling.

If any vanes are rubbing against the Optics PCB, they must be repositioned (see page K.9) before performing this adjustment. Similarly, all repair work on Optics PCBs, keys, and hammers, must be completed and vanes checked for rubbing.

A suitable tool for capstan adjustment may be purchased as a standard item at a piano tuner's supply house, or fabricated by cementing a small pan-head screw into a socket driver.

To perform the adjustment, turn the capstan so the top edge of the vane is 1.46" above the top of the keybed.

Tolerance build-ups may require a setting slightly different from this specification. The solidity and playability of the keyboard interacts with the pressure system through this capstan adjustment. The hammer must not be allowed to hit the top center rail of the chassis by adjusting the capstan too high. (On some early models you'll find foam tape applied to this upper edge, which cushions the impact of a few hammers. Unfortunately this was unavoidable in this keyboard series.) On the other hand, if the capstan is too low, the key will feel mushy because it hits the front rail punching without driving the vane through its full excursion.

K.2.3 PRESSURE THRESHOLD ADJUSTMENT

Note: For diagnostic aids to threshold adjustment, see page 10-14.5.

Pressure threshold is a "dead-band" which allows you to play a key with high velocity without necessarily engaging pressure modulation. In other words, after it "bottoms out," a key must be able to take a certain amount of force without applying any pressure modulation. This force is specified as 550 grams, +/- 150 grams, for a range of 400 -700 grams.

Before leaving the factory, all -T8 keyboards are adjusted so that when a key is pressed the key and hammer are both stopped at the same time by the front rail punching and the hammer stop foam, preventing any key "bounce". This adjustment is necessary to prevent the pressure sensors from taking pressure that should be taken by the front rail punching. This adjustment can only be made by removing the keyboard (to reach the capstans) and is unlikely to be necessary outside of the factory in most cases.

To adjust pressure threshold you need a 1000-gram force gauge (SCI #Q-124), and a #8 oblong nutdriver (SCI #Q-123), which is used to turn the actuators.

Use the diagnostics in section 10-14 to facilitate pressure threshold adjustment. If diagnostic ROM is not available:

a. Select the basic program (see page 4/5.9).

b. Switch PRESSURE-MOD FREQ A on.

Pitch-bending in this way is the easiest way to discriminate whether pressure modulation is being applied or not.

Always make sure that the "foot" of the force gauge is at the very end of each key. Apply force in as perpendicular a line as possible and continually increase until the pitch starts to bend. Do not leave the gauge on a key or "hunt" for the threshold window as this will compress the foam (resulting in a lower actuator setting than required). If it measures 400 - 700 grams, check the next key. (Obviously, the closer to 550, the better).

Figure K.2.3
MEASURING PRESSURE THRESHOLD

OSCILLATOR A
SAWS
OSCILLATOR B
SYNC
FINE
SAWS
KEYBOARD
SINGLE
SPLIT
DOUBLE
UNISON/
TRACK
MODE
LINE
PRESET
RECORD

If the key is out of range, remove it and if threshold is too low, tighten the actuator (raising it). If threshold is too high, loosen the actuator (lowering it).

While the key is removed, inspect the condition of the pedestal felt, and make a note to replace if necessary, before vane heighth adjustment for that key.

Replace key (taking care to slip it under the capstan) and check pressure threshold again with one continuous downwards motion of the gauge.

Check frequently that the gauge is zeroed.

K.2.4 KEY DIP SPECIFICATION

Key dip is the difference between the height of the key front at rest (approximately 2.2 inches above the bottom panel) and when normally pressed, contacting the front rail punching, without engaging pressure (1.8 inches). There is no single adjustment for key dip, although correct key dip is an indication of proper adjustment of other key parameters.

K.3 KEYBOARD REPAIRS

This section gives procedures for repositioning vanes, replacing hammers, and replacing keycaps.

K.3.1 VANE REPOSITIONING

NOTE: See note on page K.12 for modification to prevent vanes from rubbing.

If a vane is rubbing against an optics PCB, the key vane must be removed and repositioned on the hammer assembly for adequate clearance. CAUTION: Do not trim the curved edge of the vane.

If the anti-warp brackets are not installed, it is best to reposition vanes when the -T8 has been turned on long enough to heat up, as warpage due to heat tends to raise the back of the back rail, moving the optic sensors closer to the vanes. Repositioning the vanes while the -T8 is hot minimizes the chances of the vanes rubbing again.

To reposition the vane, carefully remove from hammer, trim the straight edge (which faces away from the optics PCB), then glue back on.

After repositioning vanes, check for minimum clearance of 0.050" between each vane and PCB. Use a small object with no sharp edges with a 0.05" dimension. (SCI# M-408 tie wrap conveniently meets this specification.)

K.3.2 REPLACING HAMMERS

First, remove the key. Hammers are attached to the rail by a single screw driven through the hammer hinge. To get access to this screw, loosen or remove the Optic board. (This may require removal of the keyboard.)

When installing the new hammer, look for the notch in the hammer rail.

An easier method of replacing hammers, in many instances, is to remove the entire hammer rail, which is held to the keybed by 4, 5, or 6 wood screws. Care must be taken not to damage other hammers when removing these screws. Before replacing the hammer rail, check for wood chips and debris in the hammer rail channel.

K.3.3 REPLACING KEY CAPS

1. To remove the key covering, place a flat iron at low heat (with a damp cloth between the key and the iron) on top of the key for approximately one minute (to make steam).

2. Separate the cap from the key using a sharp short-bladed knife. Starting at the back of the cap, gently pull the knife towards the front of key, being careful not to pull excess grain. If deep grain pull-out results, fill with plastic wood and sand smooth.

3. The same procedure applies for removing the front covering. Insert the knife at the bottom edge and gradually work the knife up behind the covering.

4. File the tops of the keys flat, being careful that the top surface remains square. If careless top-surfacing results in the tops not being square to the sides, there will be a problem when re-installing the keys. Out-of-square key tops will not level properly, which can result in costly wood repair or replacement of the keyboard.

5. Apply Raffi & Swanson #7195 cement (supplied by Pratt Read & Company, Central, N.C.) on the top of the key surface with a 1" paint brush. Place the new key covering on the cement-covered key and let it set for approximately one minute to allow the glue to flash-off and become tacky.

6. Place a metal or wood caul (flat piece of metal or wood 6" long x ¼" thick x 1" wide) on top of the covering. Place two clamps--one at the center of the head and the other 3/4" from the rear of the cap.

7. Leave the covering clamped for about five minutes. Remove the clamps and let the key cure for about twenty minutes before finishing.

8. File the side of the key covering flush to the side of the key (keeping it square), and polish it smooth.

NOTE: Mix #7195 Raffi & Swanson Cement with one part lacquer thinner and two parts cement. If used without thinning, the cement will take longer to cure and will in most instances result in showing sinks in the covering, which is not acceptable.

K.4 REMOVING KEYBOARD

The keyboard does not have to removed to remove the keys or to gain access to the pressure boards. It usually must be removed to gain access to either optics board PCB 7 or 8.

Note: If the -T8 is of later manufacture, it may be possible to remove the keyboard without performing steps 5 and 6 below. (These two steps allow side-to-side movement when the fit is especially tight.)

1. Remove top panel (see page O-20).

2. Raise boards (see page O-21).

3. Disconnect the ribbon cable that runs from PCB 3 (J301) to PCB 9 (J901). PCB 9 is mounted to the back of PCB 7.

4. Remove the control panel (see page 1/2-12).

5. Remove the side panels (see page 1/2-13).

6. Remove the wheel box (see page 1/2-13).

7. Detach the wooden front rail by removing nine screws along the front of the bottom edge. Tilt out rail and set aside in a safe place. (When installing this rail it may be easier to locate the left side first, then slide the right side in.)

8. The keybed is held to the chassis by three rows of five screws, plus the two front feet (not the two back ones). Remove these 17 screws.

9. If warpage has been a problem, there may be an additional row of five screws along the back rail, or an additional; bracket may have been installed (see next page).

10. Slide the keyboard out of the front of the chassis.

K.4 MODIFICATION TO CORRECT WARPAGE

As this manual goes to press, a modification kit is being prepared to correct warpage of the keyboard, particularly as this affects the optics.

For more information, please contact the Service Department.

Instructions are included with each kit. After installing the modification, insert the instructions beginning on the next page.

The parts for performing this modification, which consists of installing two optic board support brackets, are provided in Sequential kit #UD1008-1.

REQUIRED HARDWARE:

1 support bracket, 14½"long (MW008-13)
1 support bracket, 9½"long (MW008-14)
5 #6 x 3/8" sheetmetal screws

TOOLS REQUIRED:

1 phillips head screw driver
1 3/8" drill bit
1 power drill

PROCEDURE:

1. Remove keyboard. (If a small right-angle socket wrench is available, it may be possible to omit this step.)

2. Remove PCB 9.

3. Remove screws from PCB's 7 and 8.

4. Mount the brackets, sandwiching the optic PCB's between the keyboard back rail and the brackets, using existing screws. The longer of the two brackets goes on the right hand side as you face the keyboard in playing position.

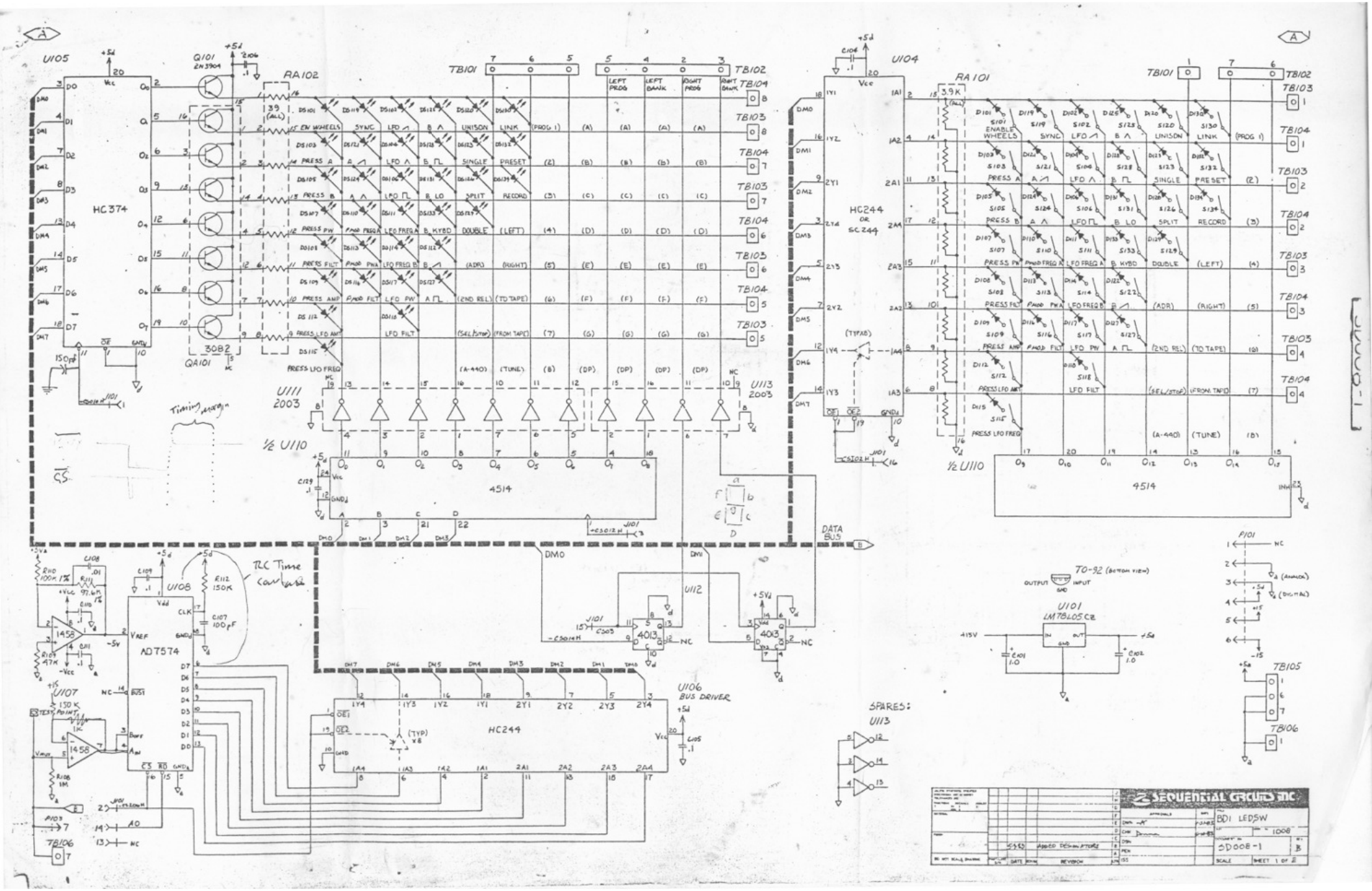
5. Reinstall PCB9, and reinstall the keyboard into the bottom panel and secure it using standard procedure.

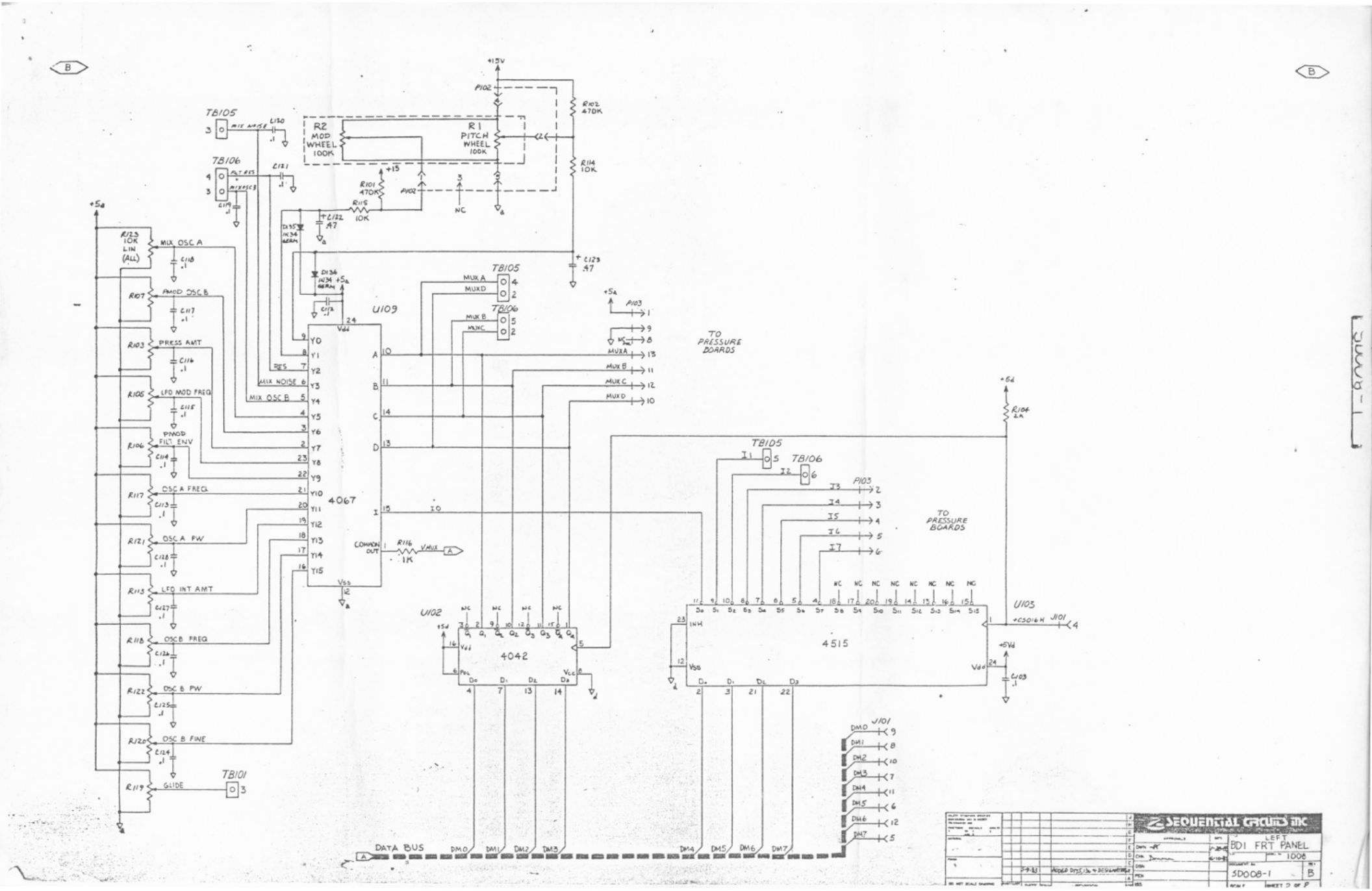
6. Using the slots in the bottom legs of the brackets as a guide, drill five holes (one at each slot location) with a 3/8" drill.

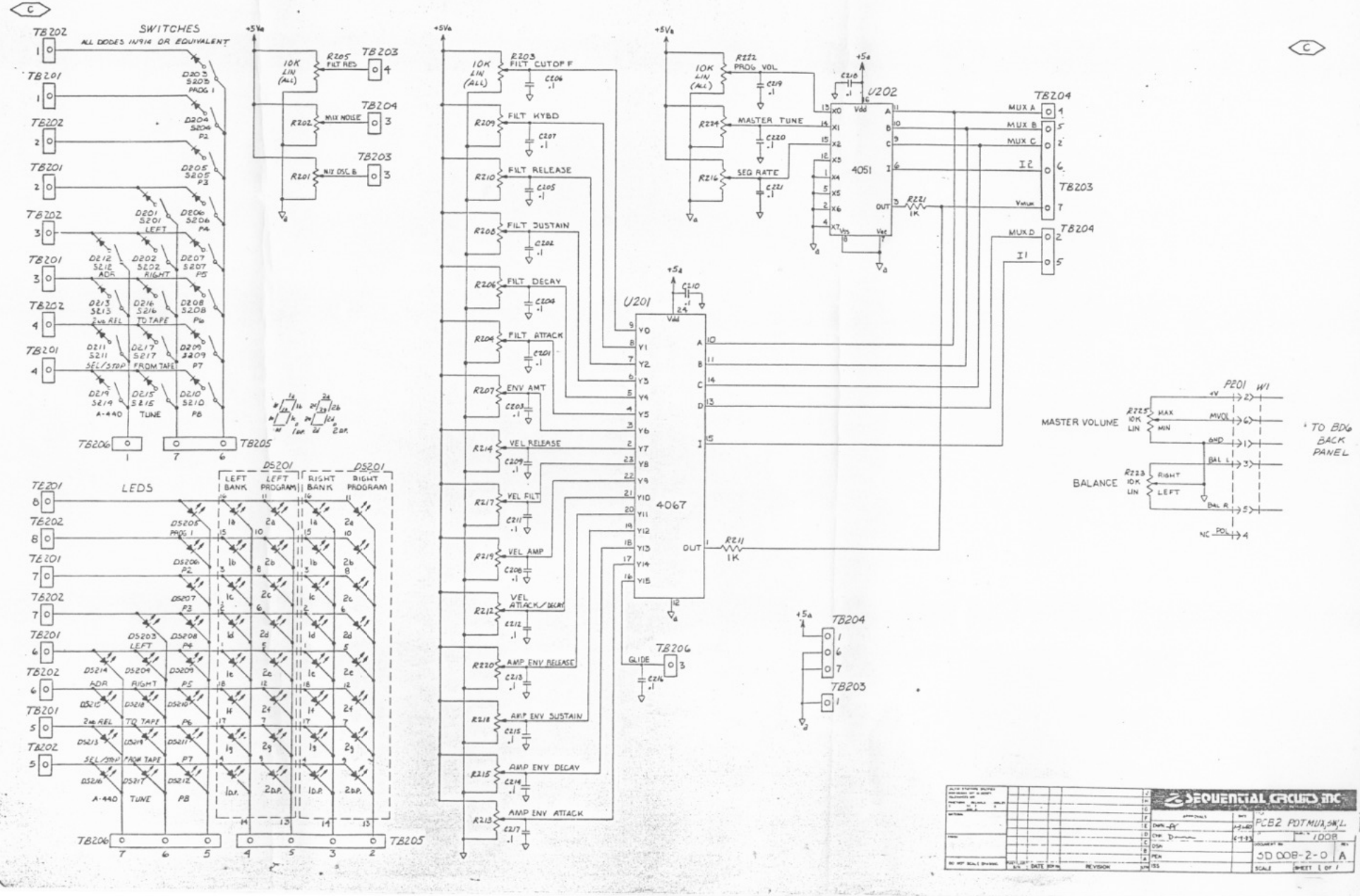
7. Secure the brackets to the bottom panel using the five #6 x 3/8" sheetmetal screws, inserting the screws from below.

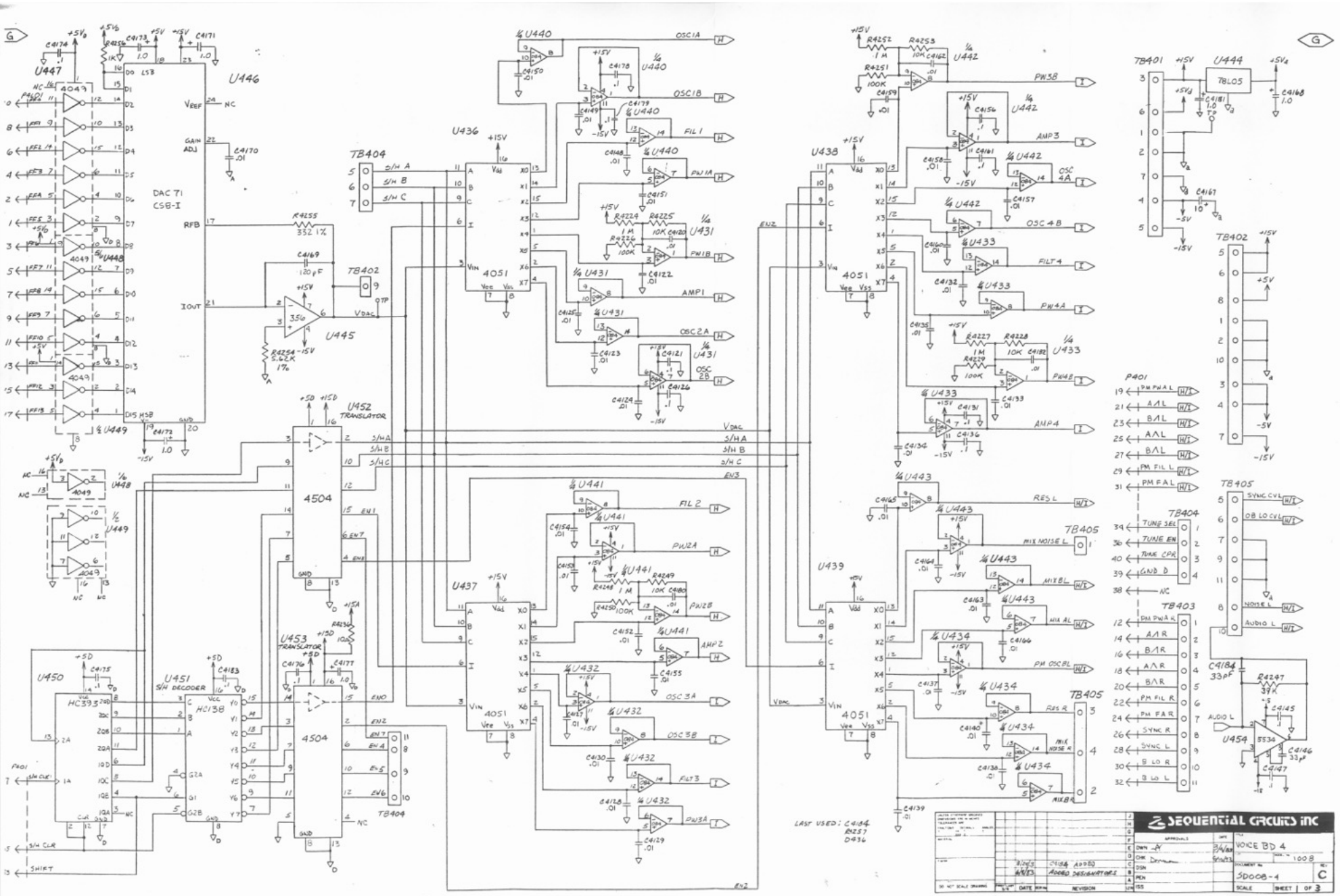
8. Check that the brackets are firmly held in place.

NOTE: Later T-8's have added two extra feet, located in the front center and rear center of the instrument, to guard against warpage. It may be advisable to install this modification if warpage of the keyboard wooden base is a problem. Additionally, owners should be advised to keep the instrument on a solid, flat surface.


U105
HC374
Q101
2N3904
RA102
TB101
TB102
TB103
TB104
LEFT PROG
LEFT BANK
RIGHT PROG
RIGHT BANK
EN WHEELS
SYNC
LFO
UNISON
LINK
PROG 1
PRESS A
LFO
SINGLE
PRESET
PRESS B
LFO
SPLIT
RECORD
PRESS PW
PMOD FREQ A
LFO FREQ A
B KYBD
DOUBLE
PRESS FILT
PMOD
LFO FREQ B
ADR
PRESS AMP
PMOD FILT
LFO PW
END REL
TO TAPE
PRESS LFO AMT
LFO FILT
SEL/STOP
FROM TAPE
PRESS LFO FREQ
A-440
TUNE
U111
2003
U113
2003
½ U110
4514
U104
HC244
OR
SC244
RA101
3.9K
ENABLE WHEELS
PROG 1
LINK
SPLIT
RECORD
LEFT
ADR
RIGHT
END REL
TO TAPE
FROM TAPE
SEL/STOP
PRESS LFO FREQ
A-440
TUNE
½ U110
4514
DATA BUS
U112
4013
4013
U108
AD7574
RC Time Constant
U107
1458
1458
U106
BUS DRIVER
HC244
SPARES:
U113
TO-92 (BOTTOM VIEW)
OUTPUT
INPUT
GND
U101
LM78L05CR
P101
TB105
TB106
SEQUENTIAL CIRCUITS INC.
BD1 LEDSW
5D008-1
SHEET 1 OF 2


+15V
P102
R102 470K
R2 MOD WHEEL 100K
R1 PITCH WHEEL 100K
R114 10K
R101 470K
R115 10K
C122 .47
C123 .47
TB105
TB106
MIX NOISE SE
MIX OSC B
C130
C131
C119
D135 1N34 GERM
D136 1N34 GERM
+5d
R123 10K LIN (ALL)
MIX OSC A
C118
R107
PMOD OSC B
C117
R103
PRESS AMT
C116
R105
LFO MOD FREQ
C115
PMOD FILT ENV
R106
C114
R117
OSC A FREQ
C113
R121
OSC A PW
C128
R113
LFO INT AMT
C127
R118
OSCB FREQ
C126
R122
OSC B PW
C125
R120
OSC B FINE
C124
R119
GLIDE
TB101
U109
4067
RES
MIX NOISE
MIX OSC B
COMMON OUT
R116 1K
VMUX
MUX A
MUX D
MUX B
MUX C
P103
TO PRESSURE BOARDS
R104 2K
U102
4042
U103
4515
+5016H
J101
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DATA BUS
SEQUENTIAL CIRCUITS INC.
LEFT
BD1 FRT PANEL
1008
SD008-1
B
SHEET 2 OF 8


SWITCHES
ALL DIODES IN4914 OR EQUIVALENT
LEDS
TB202
TB201
TB205
TB206
TB203
TB204
+5Va
10K LIN (ALL)
R205 FILT RES
R202 MIX NOISE
R201 MIX OSC B
R203 FILT CUTOFF
R209 FILT KYBD
R210 FILT RELEASE
R208 FILT SUSTAIN
R206 FILT DECAY
R204 FILT ATTACK
R207 ENV AMT
R214 VEL RELEASE
R217 VEL FILT
R219 VEL AMP
R212 VEL ATTACK/DECAY
R220 AMP ENV RELEASE
R218 AMP ENV SUSTAIN
R215 AMP ENV DECAY
R213 AMP ENV ATTACK
R222 PROG VOL
R224 MASTER TUNE
R216 SEQ RATE
R221 1K
R211 1K
U201
4067
U202
4051
MUX A
MUX B
MUX C
MUX D
I2
I1
VMUX
GLIDE
MASTER VOLUME
BALANCE
MAX
MIN
RIGHT
LEFT
MVOL
BAL L
BAL R
GND
NC
POT
P201
W1
+V
* TO BD6 BACK PANEL
DS201
LEFT BANK
LEFT PROGRAM
RIGHT BANK
RIGHT PROGRAM
PROG 1
P2
P3
P4
P5
P6
P7
P8
LEFT
RIGHT
ADR
2nd REL
TO TAPE
FROM TAPE
SEL/STOP
A-440
TUNE
1 DP.
2 DP.
SEQUENTIAL CIRCUITS INC.
PCB2 POTMUX,SW'L
1008
SD 008-2-0
A
SCALE
SHEET 1 OF 1


SD008-4
SEQUENTIAL CIRCUITS INC
VOICE BD 4
SD008-4
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SCALE
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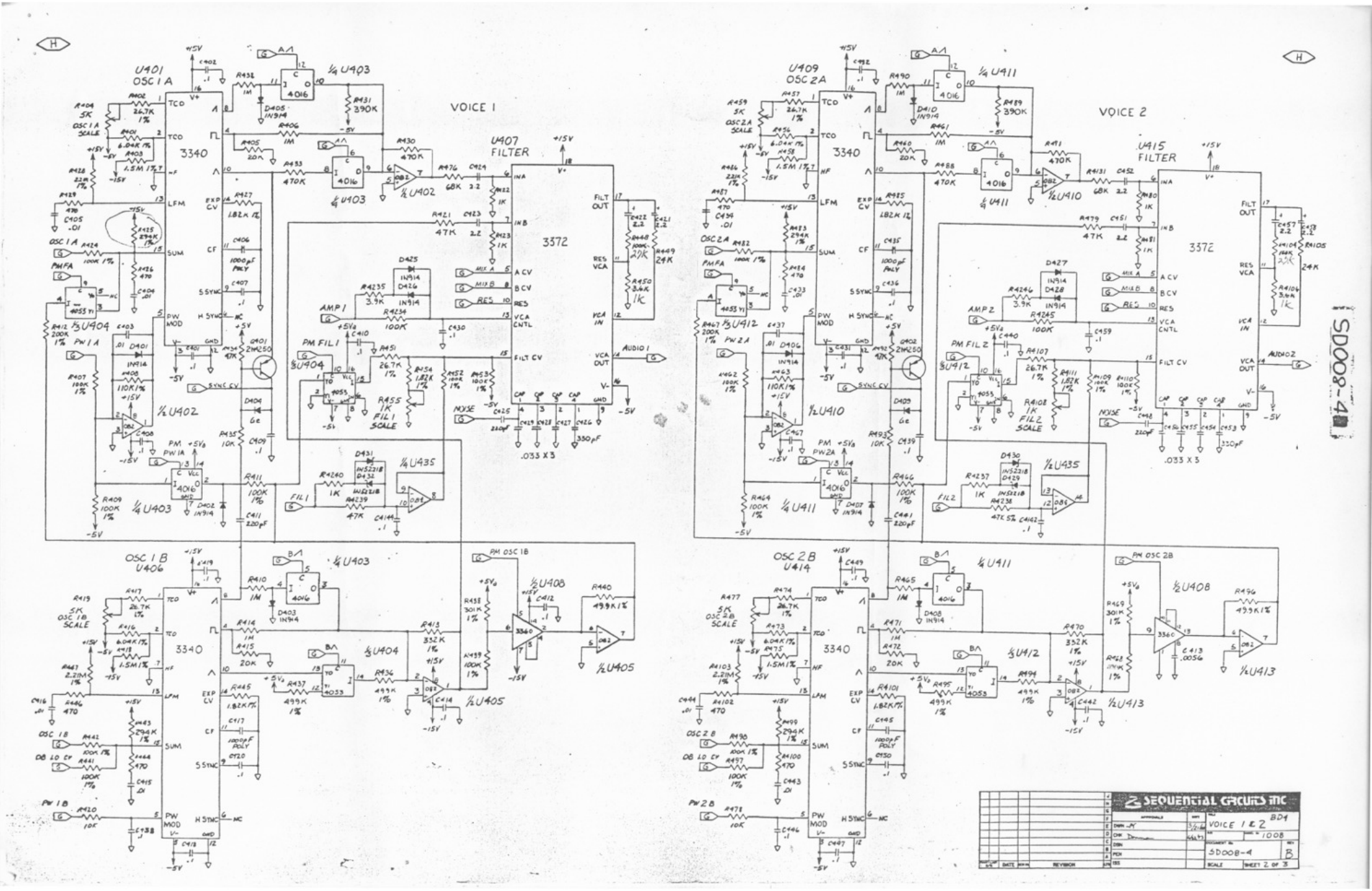
DAC 71
CSB-I
U446
U447
U445
U452
TRANSLATOR
U453
TRANSLATOR
U451
S/H DECODER
U450
U436
U437
U438
U439
U440
U441
U442
U443
U444
U445
U454
4504
4051
4049
TB401
TB402
TB403
TB404
TB405
P401
OSC1A
OSC1B
FIL1
PW1A
PW1B
AMP1
OSC2A
OSC2B
FIL2
PW2A
PW2B
AMP2
OSC3A
OSC3B
FIL3
PW3A
PW3B
AMP3
OSC4A
OSC4B
FILT4
PW4A
PW4B
AMP4
RES L
MIX NOISE L
MIXBL
MIX AL
PM OSCBL
RES R
MIX NOISE R
MIXBR
VDAC
S/H A
S/H B
S/H C
EN3
EN2
LAST USED: C4184 R4257 D436
ADDED DESIGNATORS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VOICE 2
U401 OSC 1A
U406 OSC 1B
U409 OSC 2A
U414 OSC 2B
U407 FILTER
U415 FILTER
3340
3372
OSC 1A SCALE
OSC 1B SCALE
OSC 2A SCALE
OSC 2B SCALE
PW 1A
PW 1B
PW 2A
PW 2B
PM FIL 1
PM FIL 2
AMP 1
AMP 2
FIL 1 1K SCALE
FIL 2 1K SCALE
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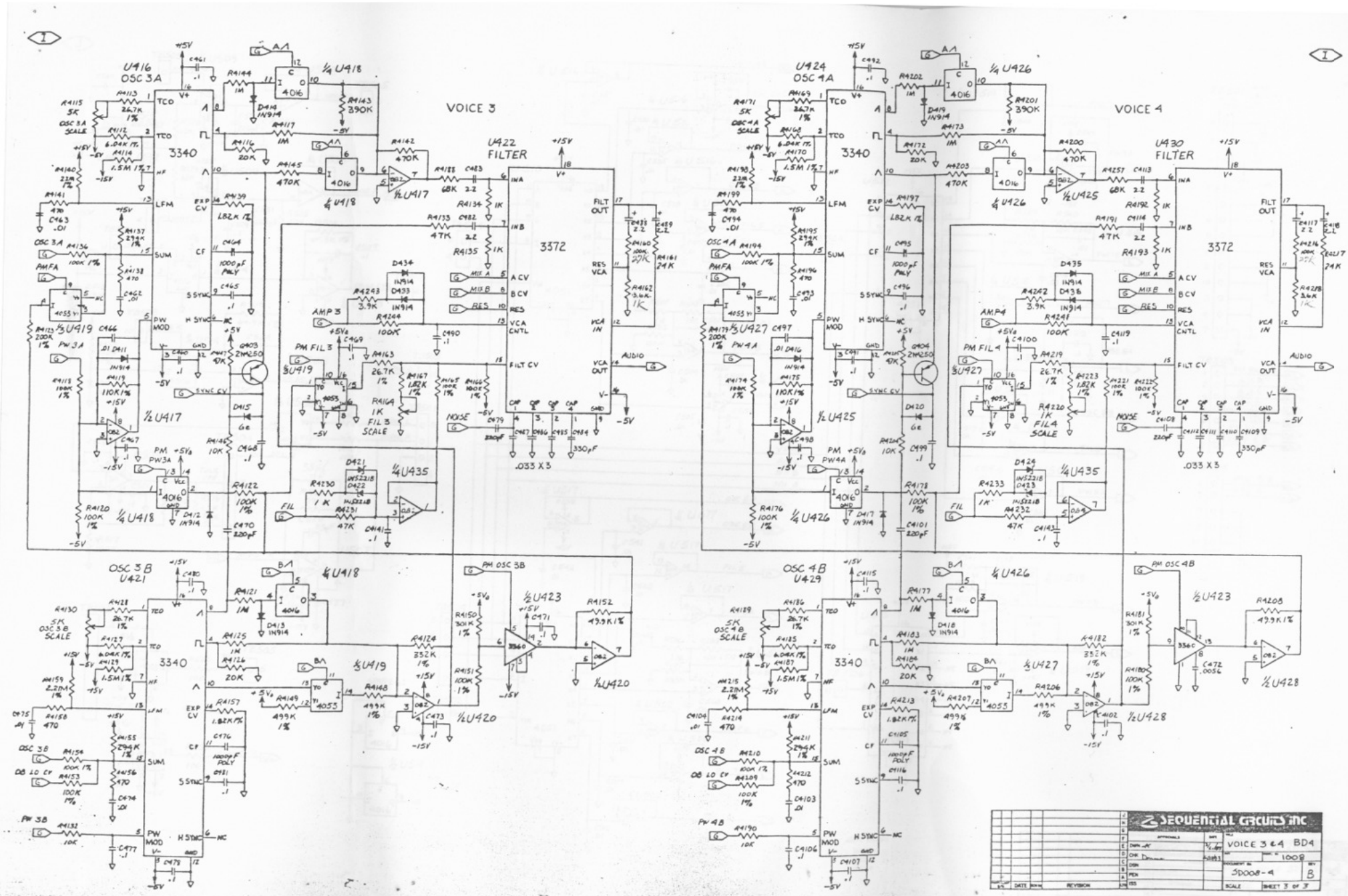
SYNC CV
NOISE
AUDIO 1
AUDIO 2
SEQUENTIAL CIRCUITS INC
VOICE 1 & 2
5D008-A
SHEET 2 OF 3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VOICE 4
U416 OSC 3A
U424 OSC 4A
U422 FILTER
U430 FILTER
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OSC 3B U421
OSC 4B U429
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VOICE 3 & 4 BD
SD008-4
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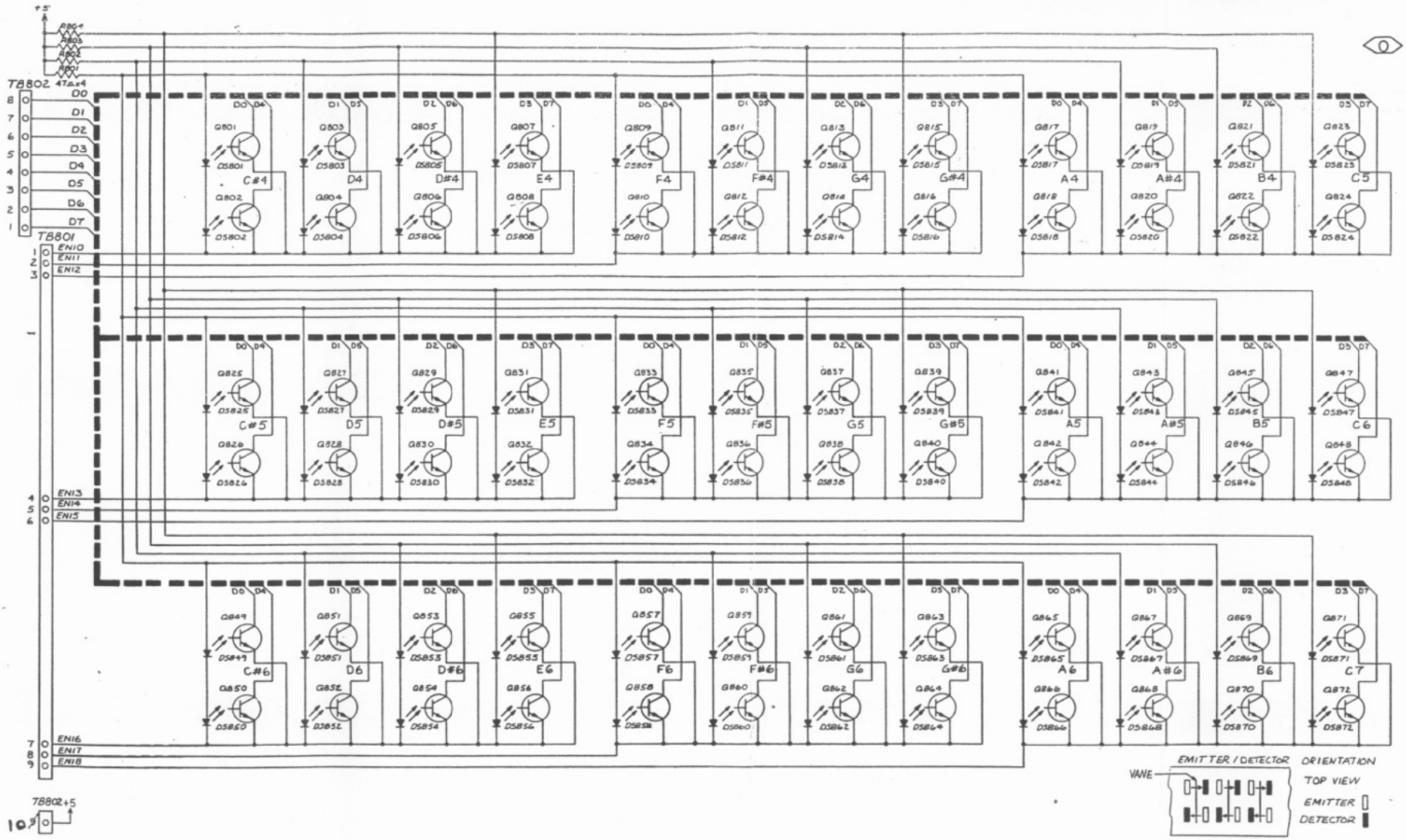

SD008-8

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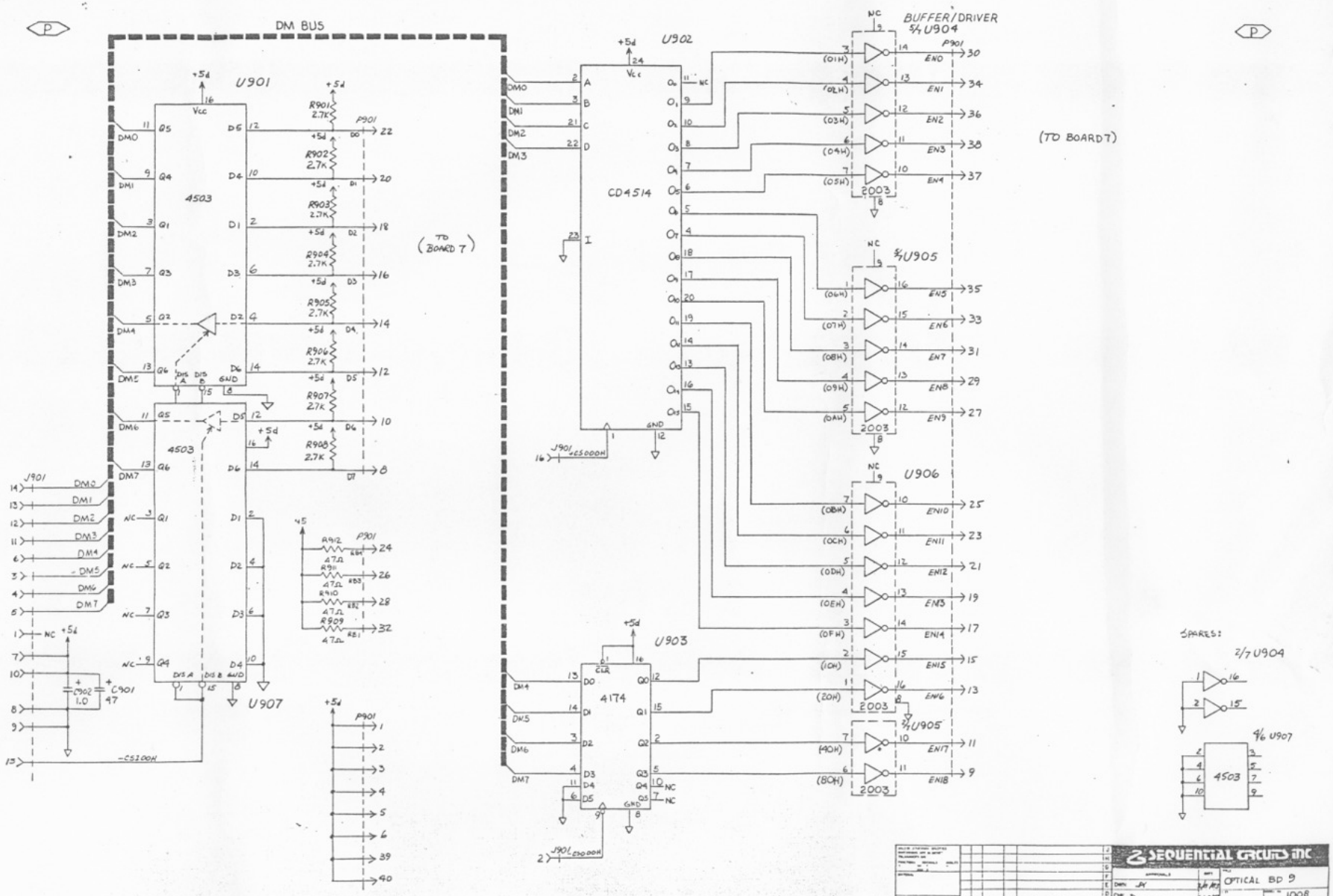
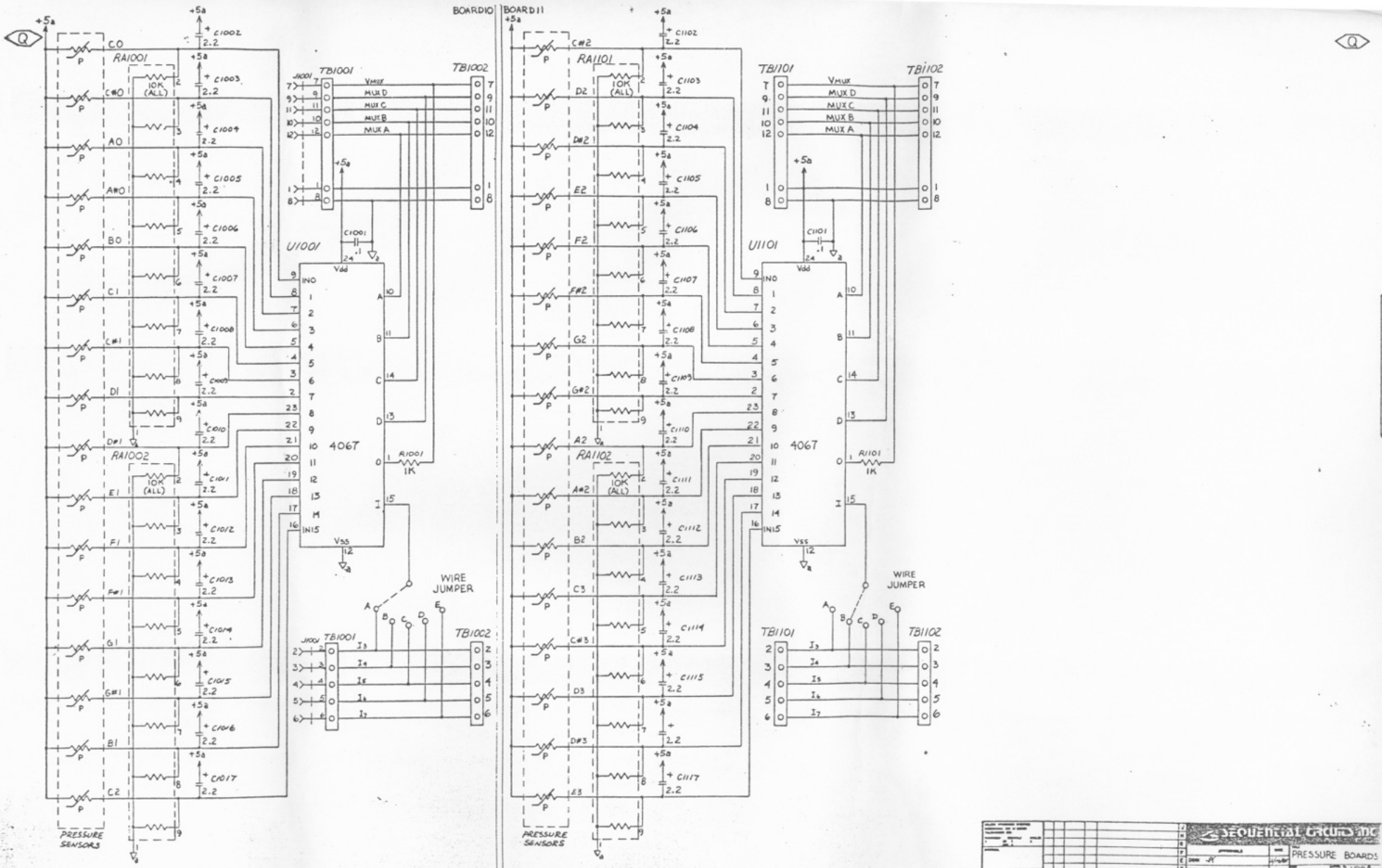
DES		DOCUMENT NO. SD008-8	REV A
PCH		SCALE	SHEET 1 OF 1
ISS			

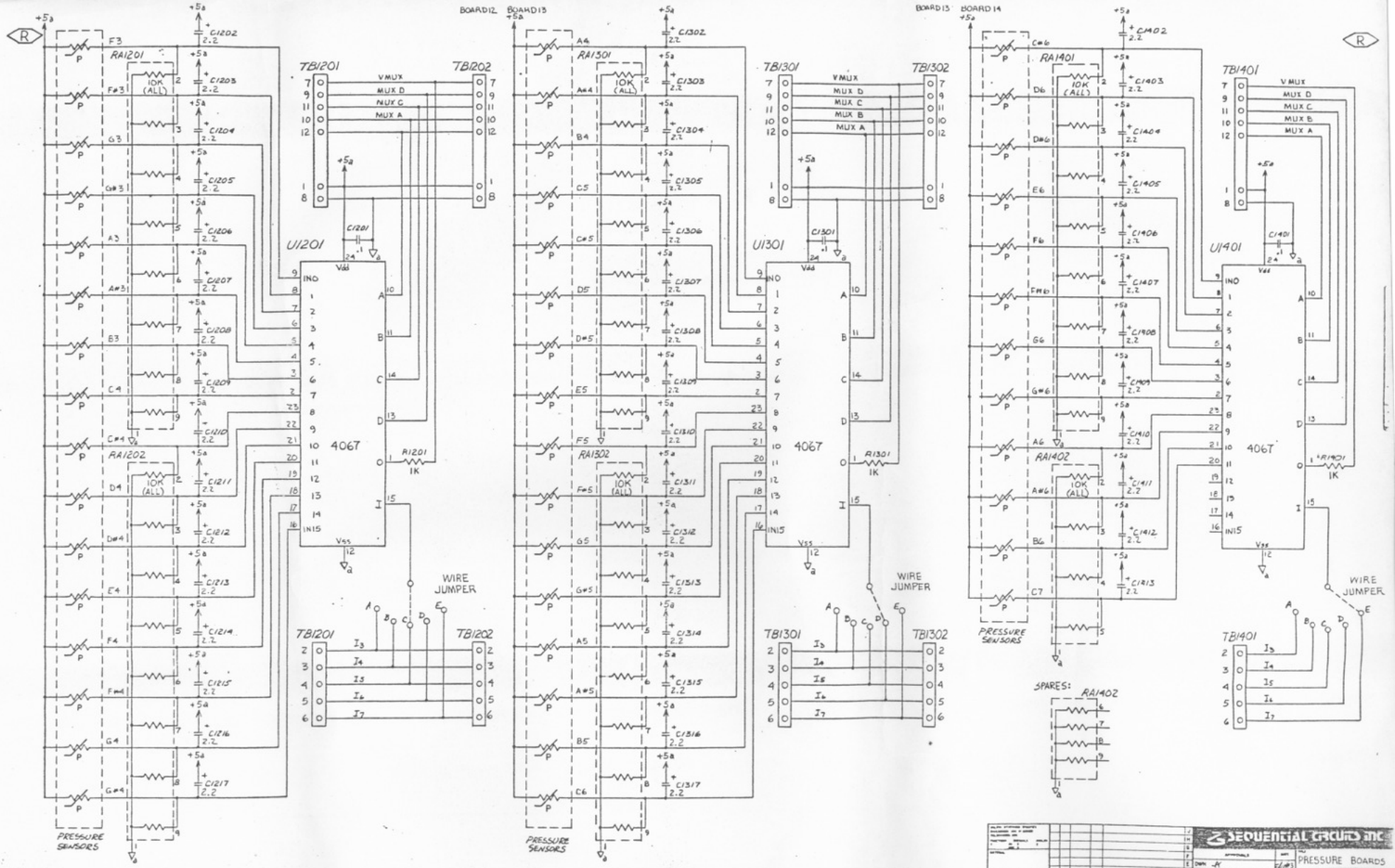

DM BUS
U901
4503
U907
U902
CD4514
BUFFER/DRIVER
5/U904
5/U905
U906
U903
4174
2003
(TO BOARD 7)
(TO BOARD7)
SPARES:
2/7 U904
9/6 U907
SEQUENTIAL CIRCUITS INC
OPTICAL BD 9
SD006-9
B

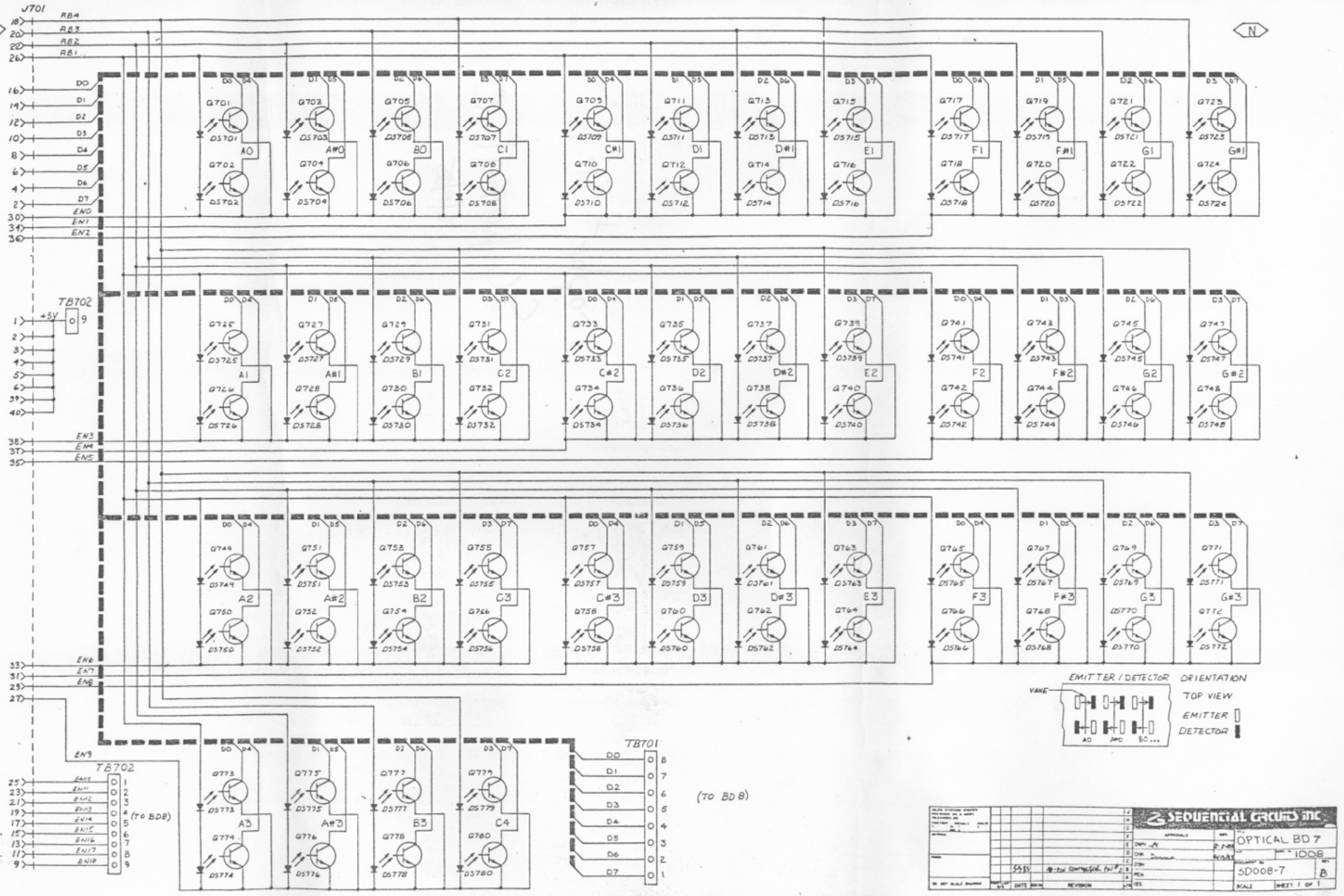


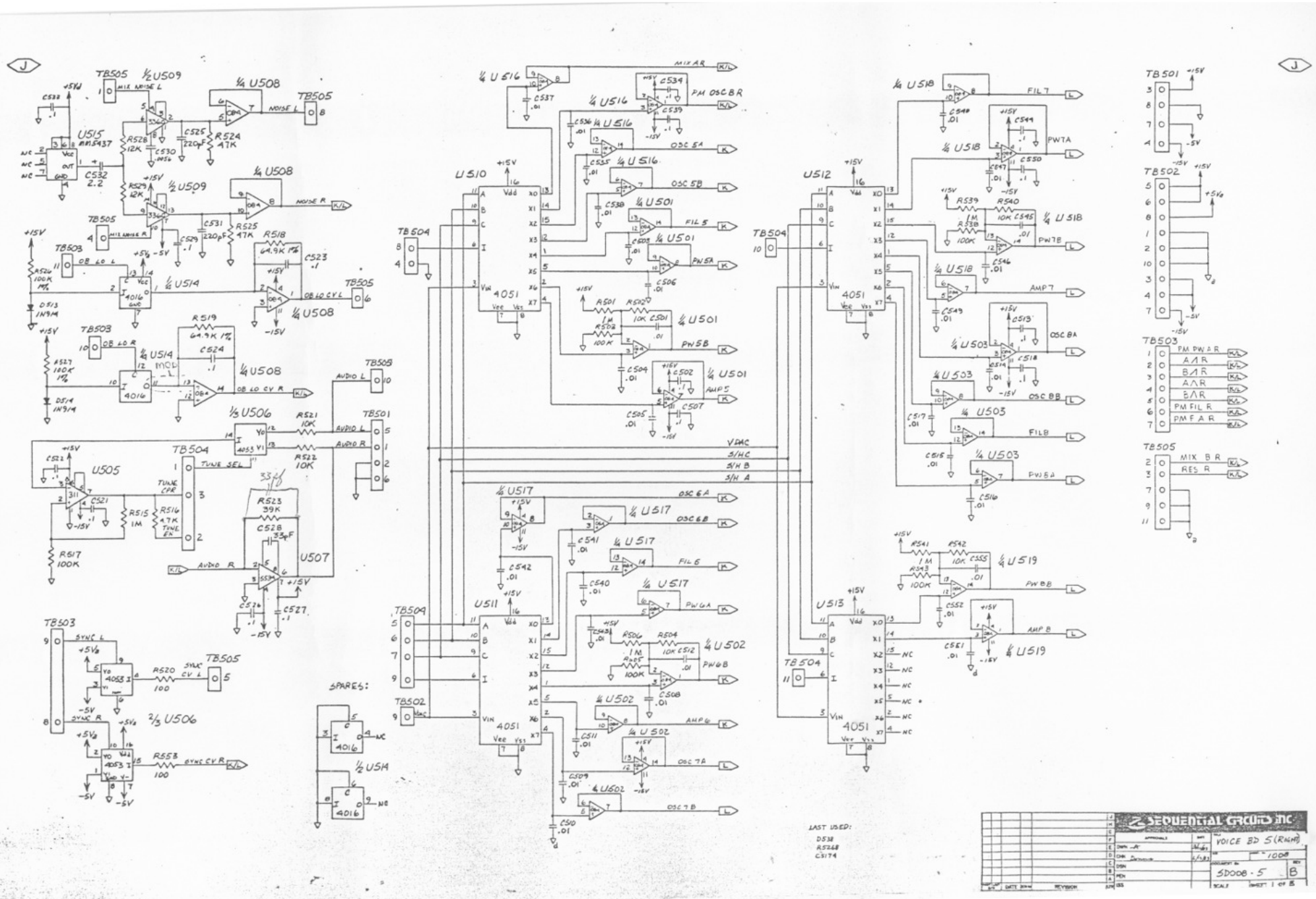
SEQUENTIAL CIRCUITS INC.

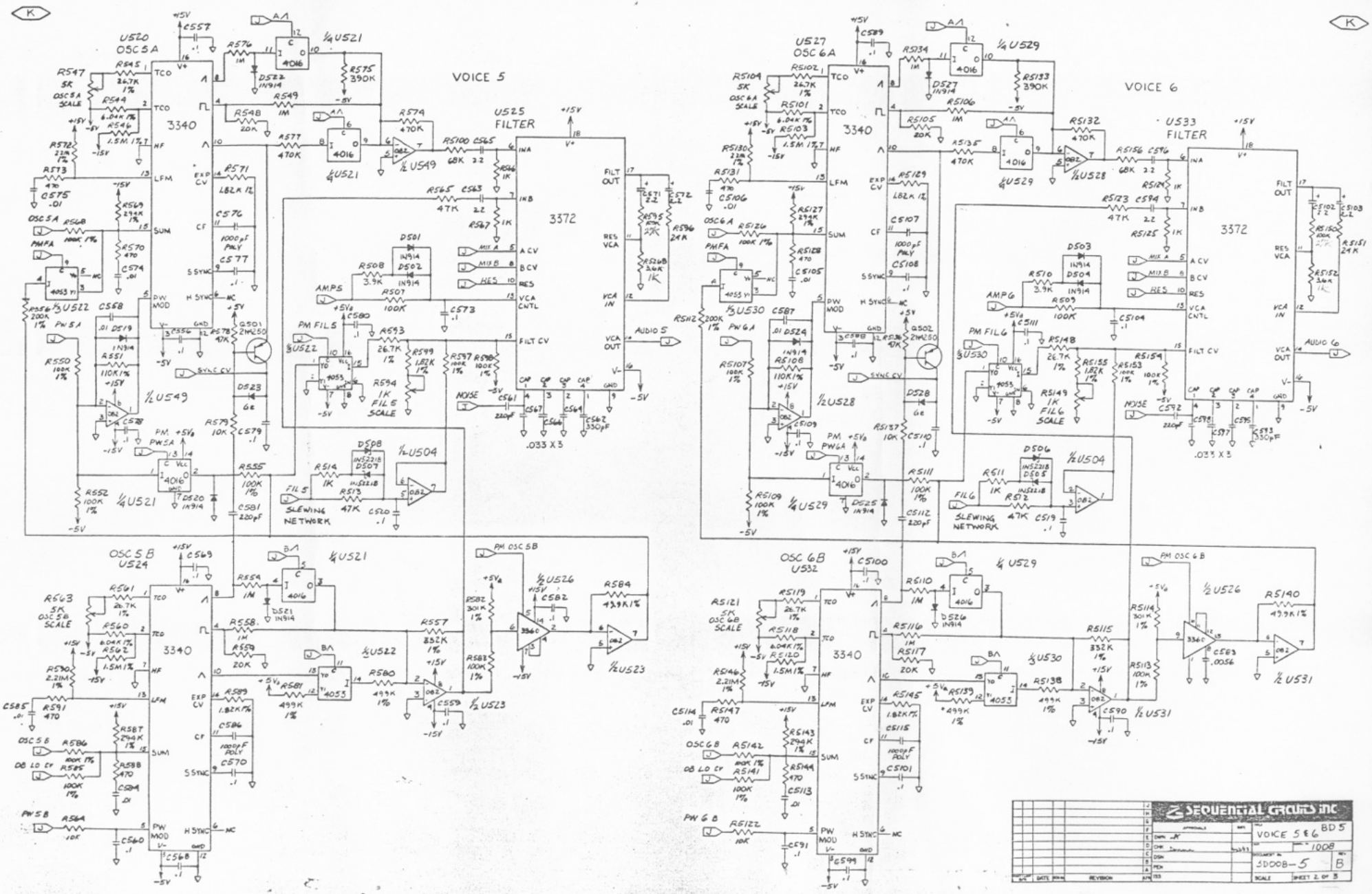
PRESSURE BOARDS

SD008-10/11


BOARD12
BOARD13
BOARD13
BOARD14
RA1201
RA1202
RA1301
RA1302
RA1401
RA1402
10K (ALL)
TB1201
TB1202
TB1301
TB1302
TB1401
VMUX
MUX D
MUX C
MUX B
MUX A
U1201
U1301
U1401
4067
WIRE JUMPER
PRESSURE SENSORS
SPARES: RA1402
SEQUENTIAL CIRCUITS INC.
PRESSURE BOARDS
5D008-12/15/14
SCALE
SHEET 1 OF 1


J701
TB702
TB701
TB702
(TO BD8)
(TO BD 8)
EMITTER / DETECTOR ORIENTATION
VANE
TOP VIEW
EMITTER
DETECTOR
SEQUENTIAL CIRCUITS INC
OPTICAL BD 7
5D008-7
8


TB505
½U509
¼U508
U515
MM5437
NOISE L
NOISE R
MIX NOISE L
MIX NOISE R
TB503
OB LO L
OB LO R
OB LO CV L
OB LO CV R
¼U514
4016
1N914
TB504
TUNE SEL
TUNE CPR
TUNE FR
U505
⅓U506
4053
AUDIO L
AUDIO R
TB501
U507
TB508
TB502
SYNC L
SYNC R
SYNC CV L
SYNC CV R
⅔U506
SPARES:
¼U516
¼U501
¼U517
¼U502
U510
U511
4051
PM OSC B R
OSC 5A
OSC 5B
FIL 5
PW 5A
PW 5B
AMP 5
FIL 6
PW 6A
PW 6B
AMP 6
OSC 7A
OSC 7B
VPAC
S/HC
S/H B
S/H A
U512
U513
¼U518
¼U503
¼U519
FIL 7
PW 7A
PW 7B
AMP 7
OSC 8A
OSC 8B
FIL 8
PW 8A
PW 8B
AMP 8
TB501
TB502
TB503
TB505
PM PW B R
A∧R
B∧R
A∨R
B∨R
PM FIL R
PM F A R
MIX B R
RES R
LAST USED:
D538
R5248
C5174
SEQUENTIAL CIRCUITS INC
VOICE BD 5 (REV H)
1008
SD008-5
B
SHEET 1 OF 5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VOICE 6
U520 OSC 5A
U527 OSC 6A
U524 OSC 5B
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U525 FILTER
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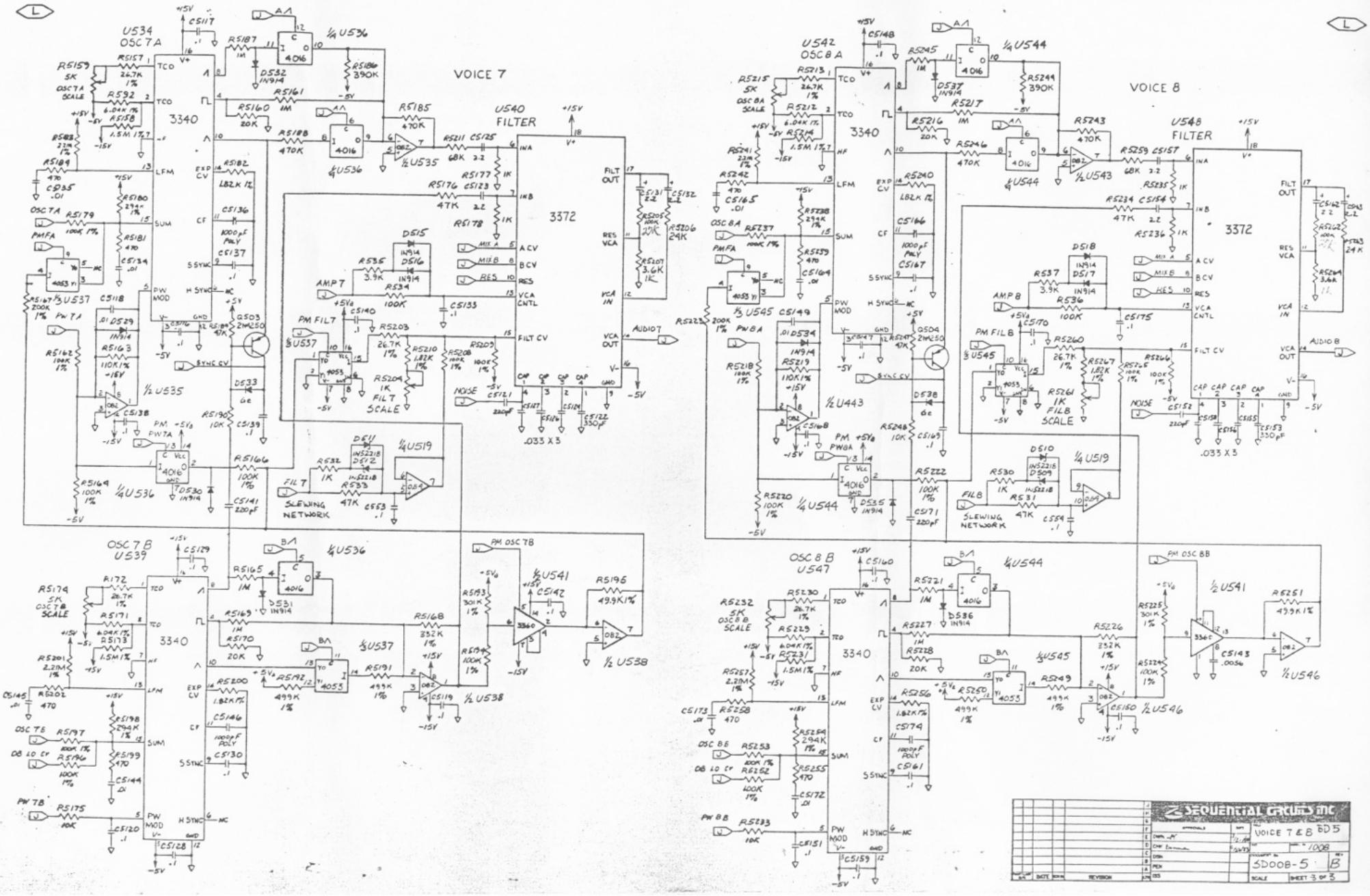
SEQUENTIAL CIRCUITS INC
VOICE 5 & 6 BD 5
5000B-5
B
SHEET 2 OF 3


VOICE 7
VOICE 8
U534 OSC 7A
U542 OSC 8A
U539 OSC 7B
U547 OSC 8B
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U548 FILTER
3340
3372
SEQUENTIAL CIRCUITS INC.
VOICE 7 & 8 BD5
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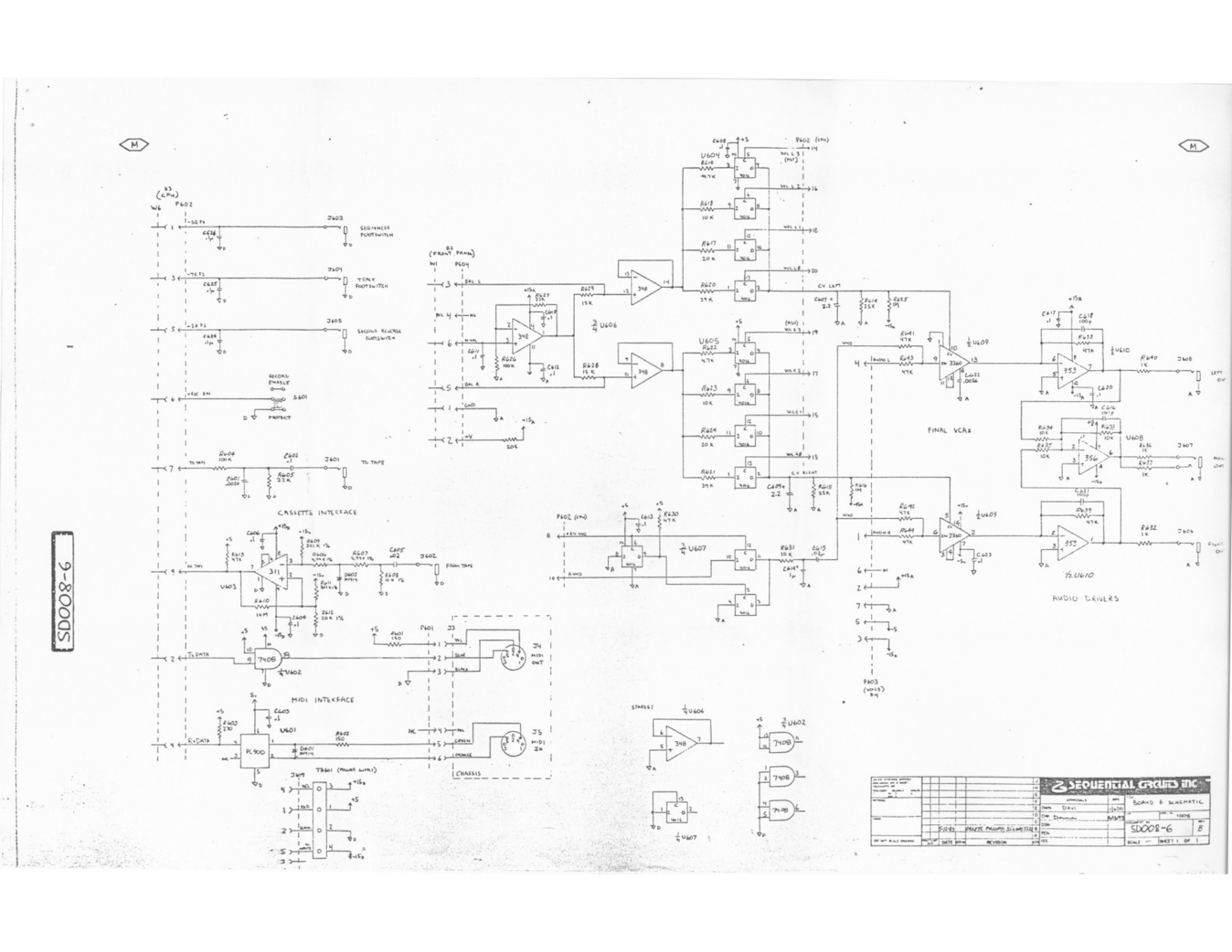
B
SHEET 3 OF 3


SD008-6
P602 (CPU)
J603
SEQUENCER FOOTSWITCH
J604
TRACK FOOTSWITCH
J605
SECOND RECORD FOOTSWITCH
RECORD ENABLE
S601
PROTECT
J601
TO TAPE
CASSETTE INTERFACE
J602
FROM TAPE
U603
MIDI INTERFACE
U601
PC900
7408
J609
73601 (POWER SWITCH)
J3
J4
MIDI OUT
J5
MIDI IN
CHASSIS
P601
P604 (FRONT PANEL)
U604
U605
CV LEFT
CV RIGHT
FINAL VCA's
AUDIO DRIVERS
P603 (VOICE BD)
SPARES:
SEQUENTIAL CIRCUITS INC.
BOARD & SCHEMATIC
SD008-6
B
SHEET 1 OF 1